TECHNICAL MANUAL

APEX™ Exciter

888-2491-001

T.M. No. 888-2491-001

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Returns And Exchanges

Damaged or undamaged equipment should not be returned unless written approval and a Return Authorization is received from HARRIS CORPORATION, Broadcast Systems Division. Special shipping instructions and coding will be provided to assure proper handling. Complete details regarding circumstances and reasons for return are to be included in the request for return. Custom equipment or special order equipment is not returnable. In those instances where return or exchange of equipment is at the request of the customer, or convenience of the customer, a restocking fee will be charged. All returns will be sent freight prepaid and properly insured by the customer. When communicating with HARRIS CORPORATION, Broadcast Division, specify the HARRIS Order Number or Invoice Number.

Unpacking

Carefully unpack the equipment and preform a visual inspection to determine that no apparent damage was incurred during shipment. Retain the shipping materials until it has been determined that all received equipment is not damaged. Locate and retain all PACKING CHECK LISTs. Use the PACKING CHECK LIST to help locate and identify any components or assemblies which are removed for shipping and must be reinstalled. Also remove any shipping supports, straps, and packing materials prior to initial turn on.

Technical Assistance

HARRIS Technical and Troubleshooting assistance is available from HARRIS Field Service during normal business hours (8:00 AM - 5:00 PM Central Time). Emergency service is available 24 hours a day. Telephone 217/222-8200 to contact the Field Service Department or address correspondence to Field Service Department, HARRIS CORPORATION, Broadcast Systems Division, P.O. Box 4290, Quincy, Illinois 62305-4290, USA. The HARRIS factory may also be contacted through a FAX facility (217/222-7041) or a TELEX service (650/372-2976).

Replaceable Parts Service

Replacement parts are available 24 hours a day, seven days a week from the HARRIS Service Parts Department. Telephone 217/222-8200 to contact the service parts department or address correspondence to Service Parts Department, HARRIS CORPORATION, Broadcast Systems Division, P.O. Box 4290, Quincy, Illinois 62305-4290, USA. The HARRIS factory may also be contacted through a FAX facility (217/222-7041) or a TELEX service (650/372-2976).

NOTE

The # symbol used in the parts list means used with (e.g. #C001 = used with C001)

MANUAL REVISION HISTORY APEX™ Exciter 888-2491-001			
Rev.	**Date**	**ECN**	**Pages Affected**
A	3/25/02		New Manual
B	1/2/03	48914	Added information about VSWR threshold and power limit functions.
C	2/25/03	49095	Added additional information about maximum peak white stretch, pages 2-20 and 3-29.
D	3/2/04	50034	Revised chapter 3 to reflect version 4.4 software and added troubleshooting tables to chapter 5. They are Table 5.1 on page 5-10, Table 5-2 on page 5-11, and Figure 5-5 on page 5-12 through Figure 5-8 on page 5-15.
E	6/2/05	51460	Revised to reflect version 5.4 software. Added PowerCD transmitter to list on page 3-26. Added asymmetrical STF information on pages 3-29 and 5-12. Revised serial setup screens 1/3 and 2/3 on pages 3-27 and 3-28. Added serial setup screen 3/3 on page 3-39. Added Loading Software on page 5-10.
F	2/16/07	54277	Reprinted book, Print driver changed symbol font to courier font, corrected that error. Changed Figures 4-2, 4-7, 4-8, 4-9. External I/O Setup Screen section, redefined Exciter Active and Equalizer Reset status input per new information received. Both inputs are on the same status input pin. Added Label for AC power switch, Figures 1-1 and 2-1. Pages 2-3 to 2-8. Pages 2-3 to 2-13 and Figure 4-1, removed references to IPA RTAC feedback. Figures 3-2 through 3-5. Designed new flow chart for exciter GUI display screens. Heading 4.4.3, PLL Board - A4, Pages 4-11 to 4-15, changed description to reflect new PLL board (part number 901-0121-061). Figure 5-4, Exciter Wiring Diagram. Redrawn to reflect new PLL board. Heading 5.1.3, Measuring and Setting Pilot and PLL Board Frequencies. Rewritten to reflect new PLL board. Table 5-4 Analog Tray RF Input and Output levels. Changed 2nd LO output jacks to J5 and J6 per new PLL board. Chapter 7, Parts Lists. Changed PLL board part number to that of new PLL board (901-0121-061). Added Appendix A, Exciter GUI Screen Captures
G	5/31/07		Corrected master pages for Appendix A

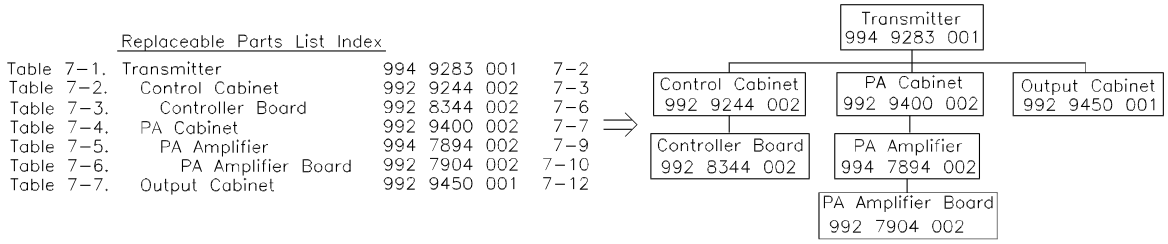
WARNING: Disconnect primary power prior to servicing.

MANUAL REVISION HISTORY APEX™ Exciter 888-2491-001			
Rev.	**Date**	**ECN**	**Pages Affected**
G	5/8/07	54782	Page 3-18, 8th line from the bottom, changed the sentence "This test is performed, while observing the exciter RF output on a spectrum analyzer, to check filter tuning." to read "Filter tuning is checked with RTAC correction bypassed, while observing the exciter RF output on a spectrum analyzer." Page 4-10, Figure 4-5, corrected frequency range or VHF filters (54-83 MHz to 54-88 MHz) and (174-213 MHz to 174-216MHz). Page 5-12, Table 5-1, changed variable on first line to EEPot (43.048 MHz Osc. adjust) to (43.048 MHz Osc. PLL adjust) Page 5-15, Figure 5-7, added page numbers to "Check Mute input status to ---" block and "Power limit should be ---" block. Page 5-17, Figure 5-9, removed "RTAC Lin IPA" from the upper left block (Is the exciter RTAC ----)
G1	6/16/09		Modified Table 1-3 on page 1-5, removed reference to FCC from Co-Channel DTV to DTV reference. Chapter 6, removed two notes recommending mask filter retuning for Pilot Frequency offsetsl. Removed reference to FCC from Section 6.1.1.3 "Co-Channel DTV and NTSC Transmitters" on page 6-4.

Guide to Using Harris Parts List Information

The Harris Replaceable Parts List Index portrays a tree structure with the major items being leftmost in the index. The example below shows the Transmitter as the highest item in the tree structure. If you were to look at the bill of materials table for the Transmitter you would find the Control Cabinet, the PA Cabinet, and the Output Cabinet. In the Replaceable Parts List Index the Control Cabinet, PA Cabinet, and Output Cabinet show up one indentation level below the Transmitter and implies that they are used in the Transmitter. The Controller Board is indented one level below the Control Cabinet so it will show up in the bill of material for the Control Cabinet. The tree structure of this same index is shown to the right of the table and shows indentation level versus tree structure level.

Example of Replaceable Parts List Index and equivalent tree structure:



Replaceable Parts List Index

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The part number of the item is shown to the right of the description as is the page in the manual where the bill for that part number starts.

Inside the actual tables, four main headings are used:

Table #-#. ITEM NAME - HARRIS PART NUMBER - this line gives the information that corresponds to the Replaceable Parts List Index entry;

HARRIS P/N column gives the ten digit Harris part number (usually in ascending order);

DESCRIPTION column gives a 25 character or less description of the part number;

REF. SYMBOLS/EXPLANATIONS column 1) gives the reference designators for the item (i.e., C001, R102, etc.) that corresponds to the number found in the schematics (C001 in a bill of material is equivalent to C1 on the schematic) or 2) gives added information or further explanation (i.e., “Used for 208V operation only,” or “Used for HT 10LS only,” etc.).

Inside the individual tables some standard conventions are used:

A # symbol in front of a component such as #C001 under the REF. SYMBOLS/EXPLANATIONS column means that this item is used on or with C001 and is not the actual part number for C001.

In the ten digit part numbers, if the last three numbers are 000, the item is a part that Harris has purchased and has not manufactured or modified. If the last three numbers are other than 000, the item is either manufactured by Harris or is purchased from a vendor and modified for use in the Harris product.

The first three digits of the ten digit part number tell which family the part number belongs to - for example, all electrolytic (can) capacitors will be in the same family (524 xxxx 000). If an electrolytic (can) capacitor is found to have a 9xx xxxx xxx part number (a number outside of the normal family of numbers), it has probably been modified in some manner at the Harris factory and will therefore show up farther down into the individual parts list (because each table is normally sorted in ascending order). Most Harris made or modified assemblies will have 9xx xxxx xxx numbers associated with them.

The term “SEE HIGHER LEVEL BILL” in the description column implies that the reference designated part number will show up in a bill that is higher in the tree structure. This is often the case for components that may be frequency determinant or voltage determinant and are called out in a higher level bill structure that is more customer dependent than the bill at a lower level.

WARNING: Disconnect primary power prior to servicing.

HARRIS Broadcast Systems Division
P.O. Box 4290, QUINCY, IL 62305

PARTS ORDER FORM

HARRIS PHONE: 217-222-8200
HARRIS FAX: 217-222-9443

BILLING INFORMATION

CUSTOMER NAME: _____

ADDRESS: _____

_____

_____

_____

TELEPHONE NUMBER: _____

FAX NUMBER: _____

PREFERRED PAYMENT METHOD: _____

SHIPPING INFORMATION

SHIP TO: _____
(if different from billing information)

ADDRESS: _____

_____

_____

_____

TELEPHONE NUMBER: _____

FAX NUMBER: _____

SHIPPING METHOD PREFERRED: _____

FREQUENCY (If required): _____

EQUIPMENT NAME: _____

EQUIPMENT PART NUMBER: _____

EQUIPMENT SERIAL NUMBER: _____

GUIDE FOR ORDERING PARTS

Please use the following parts order form, filling is as much information as possible. The complete informaiton will allow double checking the part number for correctness or locating a substitude if the part is not available.

The equipment name, part number, and serial number will be found on the metal ID plate on the back of the unit. The serial number MUST be included for any parts ordered under warranty.

Describe the part using the description in the parts list if possible. Include the schematic information, schematic number, or number of next higher assembly. The next higher assembly is usually a 992-xxxx-00x type.

ITEM #	QTY ORD	HARRIS PART NUMBER	DESCRIPTION OF PART (PART'S NAME, DESCRIPTION, SPECIFICATION FROM PARTS LIST IF AVAILABLE)	SCHEMATIC REFERENCE REFERENCE NAME (e.g. C001, R100, etc)	ITEM USED ON (NEXT HIGHER ASSEMBLY IF KNOWN) (e.g. C001 used on 992 8025 001, SCHEMATIC 839 8099 991)	COMMENTS

WARNING: Disconnect primary power prior to servicing.

WARNING

The currents and voltages in this equipment are dangerous. Personnel must at all times observe safety warnings, instructions and regulations.

This manual is intended as a general guide for trained and qualified personnel who are aware of the dangers inherent in handling potentially hazardous electrical/electronic circuits. It is not intended to contain a complete statement of all safety precautions which should be observed by personnel in using this or other electronic equipment.

The installation, operation, maintenance and service of this equipment involves risks both to personnel and equipment, and must be performed only by qualified personnel exercising due care. HARRIS CORPORATION shall not be responsible for injury or damage resulting from improper procedures or from the use of improperly trained or inexperienced personnel performing such tasks.

During installation and operation of this equipment, local building codes and fire protection standards must be observed. The following National Fire Protection Association (NFPA) standards are recommended as reference:

- Automatic Fire Detectors, No. 72E
- Installation, Maintenance, and Use of Portable Fire Extinguishers, No. 10
- Halogenated Fire Extinguishing Agent Systems, No. 12A

WARNING

Always disconnect power before opening covers, doors, enclosures, gates, panels or shields. Always use grounding sticks and short out high voltage points before servicing. Never make internal adjustments, perform maintenance or service when alone or when fatigued.

Do not remove, short-circuit or tamper with interlock switches on access covers, doors, enclosures, gates, panels or shields. Keep away from live circuits, know your equipment and don’t take chances.

WARNING

In case of emergency ensure that power has been disconnected.

If oil filled or electrolytic capacitors are utilized in your equipment, and if a leak or bulge is apparent on the capacitor case when the unit is opened for service or maintenance, allow the unit to cool down before attempting to remove the defective capacitor. Do not attempt to service a defective capacitor while it is hot due to the possibility of a case rupture and subsequent injury.

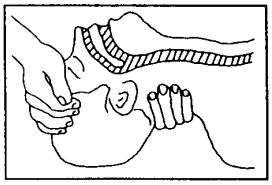
TREATMENT OF ELECTRICAL SHOCK

1. IF VICTIM IS NOT RESPONSIVE FOLLOW THE A-B-CS OF BASIC LIFE SUPPORT.

PLACE VICTIM FLAT ON HIS BACK ON A HARD SURFACE

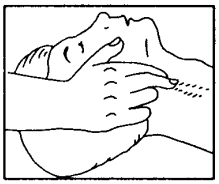
(A) AIRWAY

IF UNCONSCIOUS,
OPEN AIRWAY



LIFT UP NECK
PUSH FOREHEAD BACK
CLEAR OUT MOUTH IF NECESSARY
OBSERVE FOR BREATHING

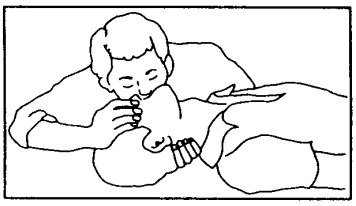
CHECK
CAROTID PULSE



IF PULSE ABSENT,
BEGIN ARTIFICIAL
CIRCULATION

(B) BREATHING

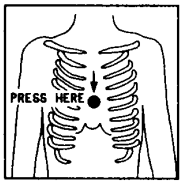
IF NOT BREATHING,
BEGIN ARTIFICIAL BREATHING



TILT HEAD
PINCH NOSTRILS
MAKE AIRTIGHT SEAL
4 QUICK FULL BREATHS
REMEMBER MOUTH TO MOUTH
RESUSCITATION MUST BE
COMMENCED AS SOON AS POSSIBLE

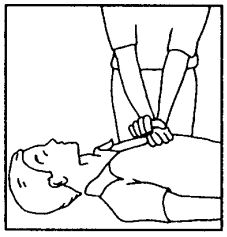
(C) CIRCULATION

DEPRESS STERNUM 1 1/2 TO 2 INCHES



APPROX. RATE OF COMPRESSIONS --80 PER MINUTE
- ONE RESCUER
- 15 COMPRESSIONS
- 2 QUICK BREATHS

APPROX. RATE OF COMPRESSIONS --60 PER MINUTE
- TWO RESCUERS
- 5 COMPRESSIONS
- 1 BREATH



NOTE: DO NOT INTERRUPT RHYTHM OF COMPRESSIONS
WHEN SECOND PERSON IS GIVING BREATH

CALL FOR MEDICAL ASSISTANCE AS SOON AS POSSIBLE.

2. IF VICTIM IS RESPONSIVE.

A. KEEP THEM WARM
B. KEEP THEM AS QUIET AS POSSIBLE
C. LOOSEN THEIR CLOTHING
D. A RECLINING POSITION IS RECOMMENDED

WARNING: Disconnect primary power prior to servicing.

FIRST-AID

Personnel engaged in the installation, operation, maintenance or servicing of this equipment are urged to become familiar with first-aid theory and practices. The following information is not intended to be complete first-aid procedures, it is a brief and is only to be used as a reference. It is the duty of all personnel using the equipment to be prepared to give adequate Emergency First Aid and thereby prevent avoidable loss of life.

Treatment of Electrical Burns

1. Extensive burned and broken skin
    A. Cover area with clean sheet or cloth. (Cleanest available cloth article.)
    B. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply any salve or ointment.
    C. Treat victim for shock as required.
    D. Arrange transportation to a hospital as quickly as possible.
    E. If arms or legs are affected keep them elevated.

NOTE

If medical help will not be available within an hour and the victim is conscious and not vomiting, give him a weak solution of salt and soda: 1 level teaspoonful of salt and 1/2 level teaspoonful of baking soda to each quart of water (neither hot or cold). Allow victim to sip slowly about 4 ounces (a half of glass) over a period of 15 minutes. Discontinue fluid if vomiting occurs. (Do not give alcohol.)

2. Less severe burns - (1st & 2nd degree)
    A. Apply cool (not ice cold) compresses using the cleanest available cloth article.
    B. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply salve or ointment.
    C. Apply clean dry dressing if necessary.
    D. Treat victim for shock as required.
    E. Arrange transportation to a hospital as quickly as possible.
    F. If arms or legs are affected keep them elevated.

REFERENCE

ILLINOIS HEART ASSOCIATION

AMERICAN RED CROSS STANDARD FIRST AID AND PERSONAL SAFETY MANUAL (SECOND EDITION)

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1 Introduction

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This technical manual contains installation, operating and maintenance procedures for the HARRIS APEX 8VSB exciter.

1.1 Organization of Technical Manual

The manual is divided into these sections:

- Section 1 - Introduction, describes the APEX exciter and lists the sections of this technical manual.
- Section 2 - Installation, describes the mounting, environmental requirements and initial setup of the exciter.
- Section 3 - Navigating the LCD Display Screens, explains how to operate the exciter.
- Section 4 - APEX Exciter Theory, explains the functioning of each part of the exciter as an aid to servicing the product.
- Section 5 - Maintenance and Troubleshooting, describes checks and test which may be used to isolate a suspected problem in the exciter.
- Section 6 - Offset Frequency Calculation, provides instructions for users who need to change the exciter to a different operating channel.
- Section 7 - Parts List, is an indexed listing of field-replaceable parts for the APEX exciter.

1.2 General Description

The APEX exciter is a low power TV transmitter signal source for the US ATSC TV broadcast service. It receives the program material to be transmitted in the form of the MPEG-2 transport stream and generates a low-level on-channel RF signal. It performs pre-corrections for signal distortions which occur in the transmitter RF power amplifiers, high power filter, and transmission line.

The APEX exciter can be installed in any Harris DTV television transmitter, or for testing, it can also be operated on any desktop or tabletop surface.

1.3 Physical Description

The APEX exciter consists of a single rack mounted chassis with the analog section available from the top of the exciter and the digital section available from the bottom.

The exciter is normally mounted in the transmitter on slides, permitting it to be extended forward out of the cabinet for service.

The exciter is 5.25" high and 19" wide to allow mounting in a 3 rack unit space in a standard 19" EIA rack. A minimum of 25" depth in the mounting rack is needed to allow space for the exciter and connecting cables.

The exciter contains a cooling blower mounted in the rear of the top side. Cooling air is drawn into the assemblies from the rear and forced over the circuits.

The top and bottom covers may be removed to provide access to the digital and analog circuit boards, however, there are no adjustments on the circuit boards. The upper side of the chassis is the analog section, and the bottom side of the chassis is the digital section.

WARNING: Disconnect primary power prior to servicing.

Figure 5-1 shows the top (analog) view and Figure 5-2 shows the and bottom (digital) view of the exciter with the covers removed. These drawings provide the names and locations of the various circuit boards of the exciter.

All system interconnections are via the rear panel, see Figure 1-1. An RS232 diagnostic port is provided on both the front and the rear panels.

Figure 1-1 APEX Exciter Rear Panel View

Refer to Figure 1-2 for a picture of the exciter. A front mounted (user interface) touch panel is provided for quick and easy configuration and operation, with minimum internal user adjustments. Extensive self diagnostics are included to aid the user.

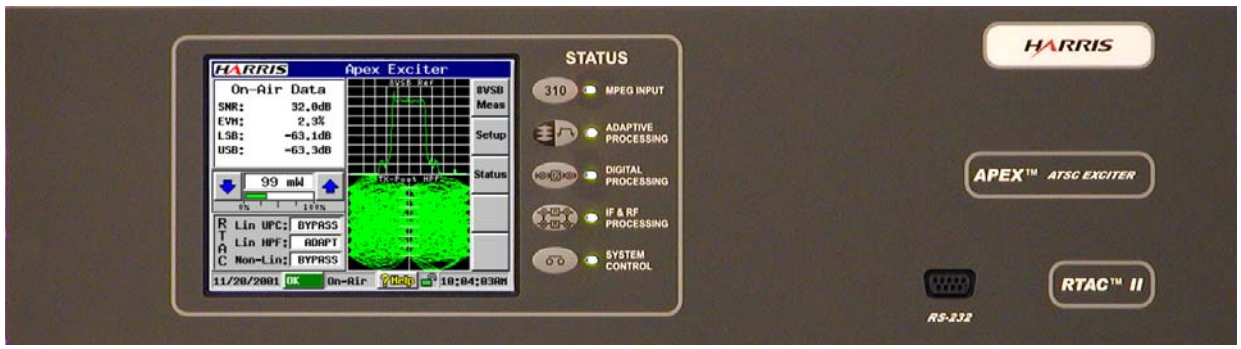

Figure 1-2 APEX Exciter Front Panel View

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1.4 Technical Overview

The exciter accepts a DTV transport data stream in SMPTE 310M (embedded clock) format. The modulation process is fully digital, with analog circuits used after the D/A converter to up-convert the IF signal to the desired channel.

The exciter RF output can be set to any VHF or UHF channel and may be adjusted to any level up to 250mW average power.

The analog chassis can accept a 10 MHz external frequency standard input via a rear-panel connector. An external standard is used whenever the user requires either greater pilot frequency precision, or a precise pilot frequency offset.

The exciter uses RTAC™ (Real Time Adaptive Correction) to monitor and manage pre correction for the transmitter system linear and nonlinear distortions, no manual correction circuits are employed. Low power RF samples from various stages of the transmitter are required by the RTAC circuits.

1.5 APEX Exciter Specifications

Specifications for the exciter are listed in Tables 1-1, 1-2, and 1-3.

Note

Specifications subject to changed without notice.

Table 1-1 Harris APEX Exciter General Specifications

Specification	**Explanation**
RF output connector	SMA, 50 ohm impedance
RF sample, from the high power filter output	SMA, 50 ohm impedance, exciter input level: -10 to 0 dBm
RF sample, from the power amplifier output	SMA, 50 ohm impedance, exciter input level: -10 to 0 dBm
RF sample, from the IPA output	Not Used
Frequency range	All VHF and UHF TV channels (2 - 69)
Transport stream input	BNC, 75 ohms, ATSC/MPEG-2, compliant to SMPTE - 310M, 19.39 Mb/s serial data
10 MHz Reference input	BNC, 50 ohms, 10 Mhz, sinusoidal, -10 to +10 dBm, > 20 dB return loss,

Table 1-2 Harris APEX Exciter Service Conditions Specifications

Specification		**Explanation**
Ambient temperature		0° to 50° celsius (32° to 122° fahrenheit)
Ambient humidity		0 to 90% relative, non-condensing
Altitude		Sea level to 10000 feet.
Physical dimensions		19 inches wide, 5.25 inches high, 24 inches deep
Weight		36 pounds
Electrical Requirements	Voltage	85-132/170-264VAC
	Current	2.4/0.75 AMPS
	Power	200 VA
	Frequency	47-63HZ
	Fuse size	T4A/250V

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Table 1-3 Harris APEX Exciter Performance Specifications

Specification	**Explanation**
Maximum power output	1 watt peak, 250 mW average
Power output range	Programable 1 to 250 mW average
Regulation of output power	1% or less
Pilot frequency stability	±200 Hz per month without PFC (precise frequency control)
	<0.5 Hz per 1% supply variation
	<50 Hz over 0° to 65° C ambient temperature range
	<100 Hz at 5 minutes during warm up
Pilot frequency offsets [1]	Per FCC 73.622 requirements, 2 millihertz resolution
Co-channel DTV to DTV	N × 6.4676909629 kHz, where N is odd (19.4030728887 per ATSC A/64)
Co-channel NTSC to DTV	-911944 Hz, NTSC visual to DTV pilot (FCC 73.622 and ATSC A/64)
Upper adjacent DTV to NTSC	5.082138 MHz, NTSC visual to DTV pilot (Per FCC 73.622 and ATSC A/64)
Response variation	< 0.2 dB, with the exciter in loopback mode
Group delay	< 2 nsec, with the exciter in loopback mode
Phase noise	Greater then -104 dBc/Hz at 20 kHz offset (ATSC A/64)
Spurious output [2]	
In band	-68 dB (-45 dB as measured in 30 kHz RBW)
Adjacent channels	-68 dB (-45 dB as measured in 30 kHz RBW)
Signal to noise ratio [3]	35 dB typical, with the exciter in loopback mode
Note 1. High-stability external 10 MHz reference required for precise frequency control.	
Note 2. Signals referenced to center of channel, at rated output, measured with 30 kHz RBW.	
Note 3. Demodulated SNR measured with Agilent 89440A/89441A/89441V vector signal analyzer.	

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2 APEX Exciter Installation

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2.1 Introduction

Exciters sold as part of a transmitter will normally have been tested in the transmitter before shipment. The exciter may be removed for shipment, to be reinstalled after the transmitter is in place. Installation is a simple process, as described in 2.2 below.

Exciters sold for retrofit into existing transmitter systems will not only require mounting and appropriate mounting hardware, but because this exciter requires three RF samples instead of the one sample of the CD-1A, additional sample cables will have to be installed.

Exciters sold for use in test facilities can either be rack mounted or operated standing on a work surface.

2.2 Installing Exciters Removed for Shipment

If an exciter has been removed for shipment, the physical mounting hardware and connecting harness should already be in place in the transmitter. Mount the exciter in its mounting slides, fasten the flexible cable retractor (if used) to the rear and connect the cables to the rear panel as marked.

The exciter should have been set up at the factory, and the settings recorded of the transmitter final test data. The information in Section 3, Operating the APEX Exciter and Section 2.6, Configuring the Exciter should be carefully studied before attempting to operate the exciter or check the exciter setup against the factory final test data.

2.3 Signal Connections

Most of the input and output connections are at the rear of the exciter, only the RS232 connections are available at the front and rear. Figure 2-1 shows the rear panel connections.

- SMPTE 310M IN (Isolated BNC) is the input connection for the MPEG-2 transport stream SMPTE-310M input signal. For best common mode rejection, this cable shield should be grounded only at the source end.

  The transport signal source, which connects to the exciter's SMPTE 310M input, must conform to the SMPTE 310M standard. The input impedance is 75 ohms. Belden 8281 or similar high-quality video cable can be used to deliver this signal to the exciter over a distance of up to 1000 feet.
- 10MHZ REF IN (BNC) is the (Optional) 10 MHz reference frequency input. It is used when precise control of the exciter's pilot frequency is required. Normal signal input range is -10 to +10 dBm. The input impedance is 50 ohms.
- HPF RF SAMPLE IN (SMA) is the input signal connector for an RF sample from output of high power filter. It is used by RTAC™ (Real Time Adaptive Correction) to correct for the linear distortions of the high power filter. Normal input signal range is +5 dBm to -30 dBm. The input impedance is 50 ohms.
- PA SAMPLE IN (SMA) is the input signal connector for an RF sample from the output of the transmitter power amplifier, taken before the HPF. It is used by RTAC™ to correct for the nonlinear distortion caused by the power amplifier. Normal input signal range is +5 dBm to -30 dBm. The input impedance is 50 ohms.

- IPA SAMPLE IN (SMA) is the input signal connector for an RF sample from the output of the transmitter intermediate power amplifier. It is used by RTAC™ to correct for linear distortions caused by all of the filters from the D/A board to the IPA output. Normal input signal range is +5 dBm to -30 dBm. The input impedance is 50 ohms.

  This input is not used on Harris transmitters since the IPA output has negligible group delay.
- RF OUT (SMA) is the on-channel RF signal output from the exciter. Output level is adjustable up to 250 mW average.
- EXC/CTRL UHF (25 Pin D) is the exciter control interface connector used to connect the UHF version of the exciter to the transmitter and the exciter switcher.
- EXC/CTRL VHF (37 Pin D) is the exciter control interface connector used to connect the VHF version of the exciter to the transmitter and the exciter switcher.
- CAN (controller area network) is a provision for the exciter to communicate with the transmitter GUI (graphical user interface) system controller.
- LAN 10Base-T is a provision for connecting the exciter to a local area network.
- RS232 (on front and rear panels of exciter) is a 9 Pin D interface connector. They are used to communicate with various computer applications. The front and rear panel connections can be programmed and used independently of each other.

2.3.1 AC Power

AC Power is applied through a standard power cord to the connector at the right side of the rear panel as shown in Figure 2-1. The AC inlet connector also contains the power switch.

The power supply will automatically select the AC input voltage in two ranges. The two ranges are 85 to 132 VAC or 170 to 264 VAC

Figure 2-1 Exciter Inputs and Outputs

2.4 Retrofitting Into Existing Transmitter System

One of the most important aspects of installing the exciter into an existing transmitter consists of providing the APEX with the appropriate feedback signals. It is impractical to discuss every possible transmitter installation, the intent of this section is to provide enough information to the systems engineer to allow him to determine the optimum feed back arrangement. The discussions below will address the most common configurations.

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2.4.1 Feed Back Requirements

The APEX Exciter accepts up to two feedback signals. They are the HPF and PA. Each sample input accommodates an input level of -10 to 0 dBm average DTV power.

The HPF sample monitors the output of the FCC Mask Filter. It uses this sample to characterize the amplitude response and group delay response of the filter. This filter can be a standard “D” Mask, “STF” (sharp tuned filter) or channel combiner. After the filter has been characterized the APEX applies pre-correction such that the response and delay have been optimized at the filter output. In addition to characterizing the mask filter, any transmission line or antenna VSWR present at the monitoring point will also be compensated.

The PA sample monitors the output of the final amplifying device. It uses this sample to characterize the AM to AM (linearity) and AM to PM (phase) distortions of the amplifier and apply pre-correction to optimize the spectrum response (adjacent channel shoulder level) at the amplifier output.

2.4.1.1 Feedback Signal Quality Requirements

The ability of the APEX exciter to correct transmitter system distortions depends on the quality of the feedback samples. Any frequency response errors introduced in the feedback system will degrade the main signal path. This will occur since the APEX compares the ideal signal in the exciter to the feedback signal presented to the rear panel. The correction algorithms, like any feedback loop, will drive the error to zero at the measurement point, which is at the rear panel. Use only a high quality 50-ohm coax such as RG223. Avoid the use of multiple lengths of cable; multiple connectors can cause response errors in the feed back path**.** Always terminate any unused ports on a coupler, splitter, combiner or other RF device. Poor EVM performance can generally be traced back to a faulty feed back path.

2.4.2 Typical Transmitter Systems Block Diagrams

The block diagrams in Figures 2-2 through 2-18 show typical RF line-ups for various transmitters. They will be helpful in determining how to configure the feedback signals. The bold lines indicate the required transmitter additions. There is also a recommended list of required materials in Section 2.7 on page 2-17.

In most cases the required couplers are already installed in the main RF path for transmitter monitoring. These couplers can be used to provide the feedback samples to the APEX exciter. In the event that a given coupler is dedicated to a transmitter function, that sample can be split into two paths using a coupler, with the output port of the added coupler connected to the transmitter function input cable and the coupled port used for the APEX feedback signal.

If a transmitter installations use multiple PA cabinets, the PA sample is taken after the PA combiner. The APEX corrects for the aggregate sum of the PA cabinets.

Some transmitter installations use multiple high power filters. In this case the HPF sample is taken after the combiner and the APEX corrects for the aggregate sum of the filters. Since there is no one sample available for the PA output, the individual samples must be combined and the aggregate sum fed back to the APEX.

2.4.3 Platinum Transmitters

Platinum transmitters can be configured with one or more PA cabinets and single or dual exciters. This gives rise to four feedback systems, as described below.

2.4.3.1 Platinum Transmitters - 1 PA Cabinet and Exciter

In the existing system, shown in Figure 2-2, the cabinet monitoring signals are taken from the PA cabinet coupler and high power filter output coupler. Each of these signals are split with directional couplers, with the coupled outputs connected to the appropriate APEX exciter feedback input, as shown in Figure 2-3.

If the cabinet and system monitoring outputs are not used, they should be terminated to prevent distortion of the APEX exciter feedback samples by the reflected signals.

The feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

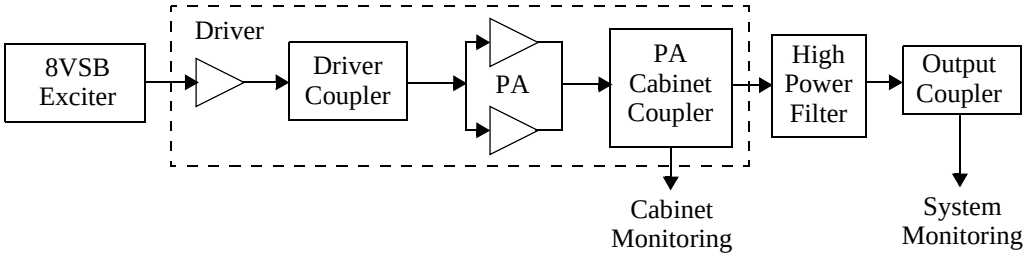

Figure 2-2 Platinum Transmitter with Single PA Cabinet

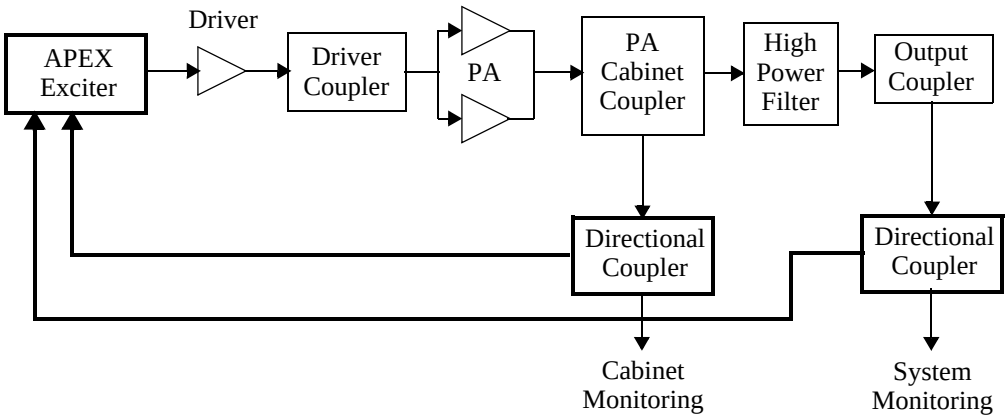

Figure 2-3 Feedback Connections for Platinum Transmitter with Single PA Cabinet

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2.4.3.2 Platinum Transmitter - 1 PA Cabinet, 2 Exciters

If the Platinum transmitter system shown above (with one PA cabinet) has dual exciters, as shown in Figure 2-4, the feedback connections are modified from the connections shown in Figure 2-3 by putting two-way, zero-phase splitters in each feedback sample line. The outputs of each splitter provide the appropriate feedback signal for each exciter, as shown in Figure 2-5.

If the cabinet and system monitoring outputs are not used, they should be terminated to prevent distortion of the APEX exciter feedback samples by the reflected signals.

The feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

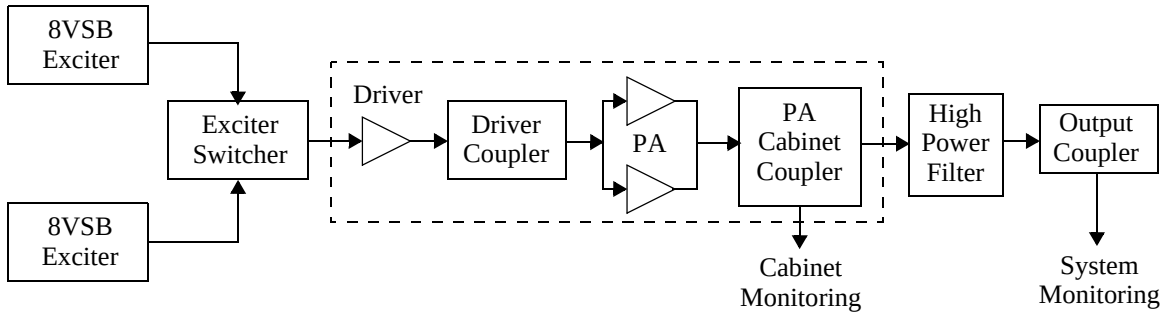

Figure 2-4 Platinum Transmitter - Single PA Cabinet - Dual Exciters

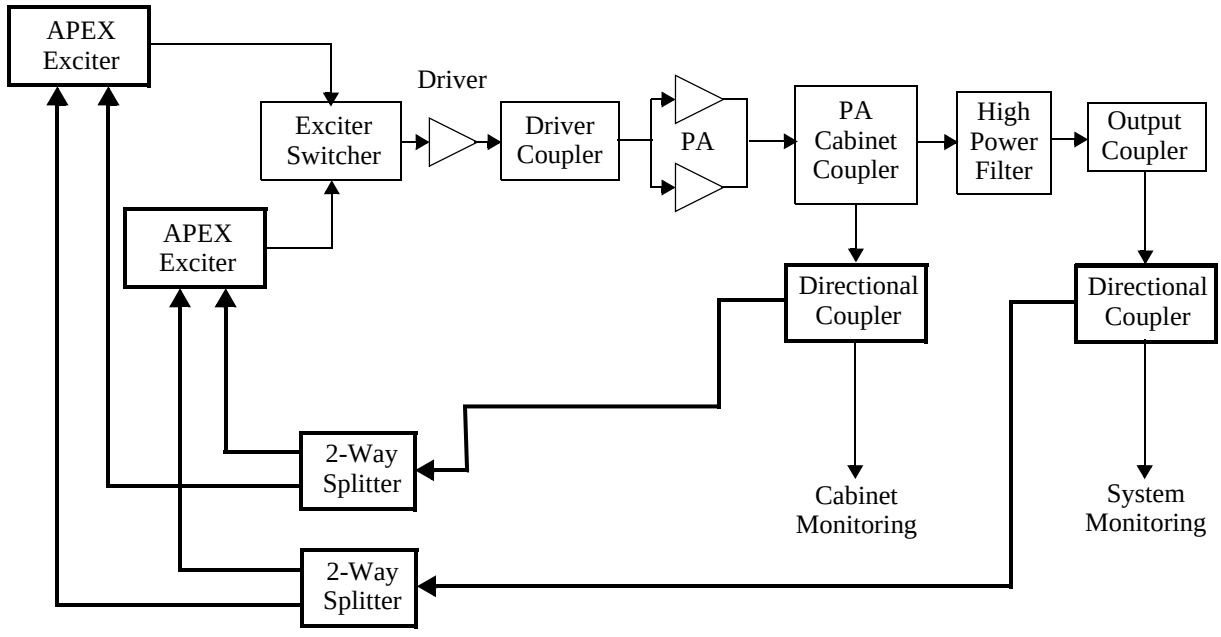

Figure 2-5 Platinum Transmitter - Single PA Cabinet - Dual APEX Exciters

WARNING: Disconnect primary power prior to servicing.

2.4.3.3 Platinum Transmitter - 2 or More PA Cabinets

When the Platinum Transmitter has two or more PA cabinets, the feedback signals are connected as shown in Figure 2-6.

- The HPF feedback sample is taken from the high power filter output coupler.
- The PA sample is taken from the cabinet combiner output coupler.
- If the transmitter system has dual exciters, feedback samples for each exciter are obtained by splitting each sample cable, as shown in Figure 2-7
- If the cabinet and system monitoring outputs are not used, they should be terminated to prevent distortion of the APEX exciter feedback samples by the reflected signals.
- The feedback signals at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The sample input power range is -10 to 0 dBm.

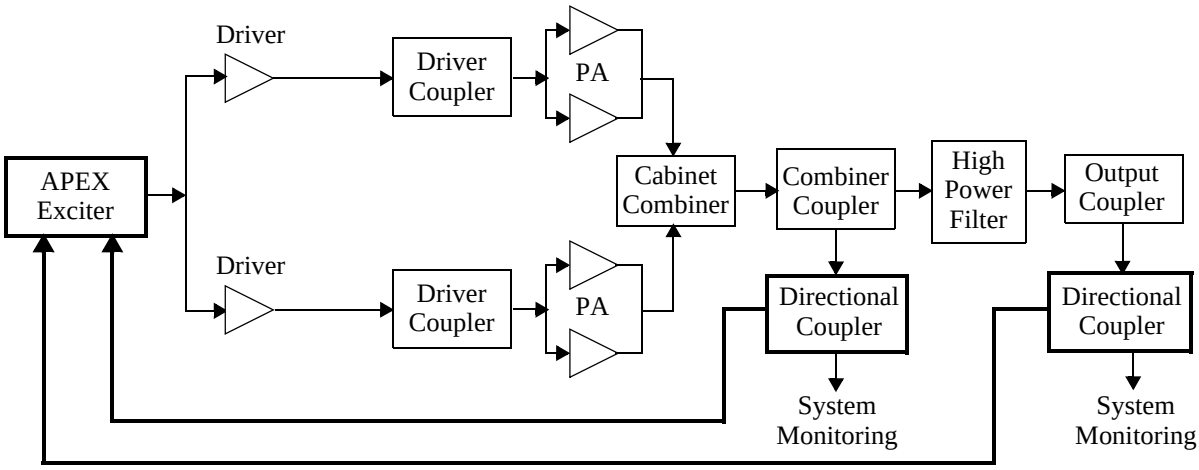

Figure 2-6 Platinum Transmitter - Dual PA Cabinets - Single APEX Exciter

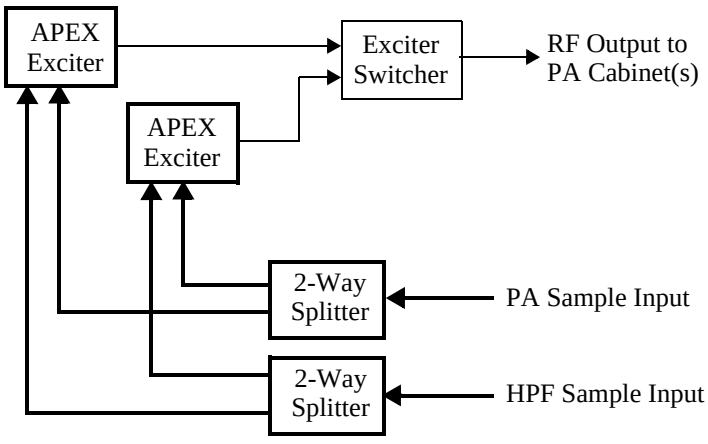

Figure 2-7 Platinum Transmitter - Showing Modification for Dual APEX Exciters

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2.4.4 Diamond Transmitters

Diamond transmitters can be configured with one or more PA cabinets and single or dual exciters. This gives rise to four feedback systems, as described below.

The Diamond configuration places the driver module in the control cabinet. The driver output feeds one to five PA cabinets. If the transmitter system has dual exciters and drivers, the driver outputs are connected to a coax relay, which connects one driver to a test load and the other to drive the PA cabinets.

2.4.4.1 Diamond Transmitters - 1 PA Cabinet and Exciter

In the existing system, shown in Figure 2-8, the cabinet monitoring signals are taken from the high power filter input coupler and high power filter output coupler. Each of these signals are split with directional couplers, with the coupled outputs connected to the appropriate APEX exciter feedback input, as shown in Figure 2-9. If the cabinet and system monitoring outputs are not used, they should be terminated to prevent distortion of the APEX exciter feedback samples by the reflected signals.

The feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

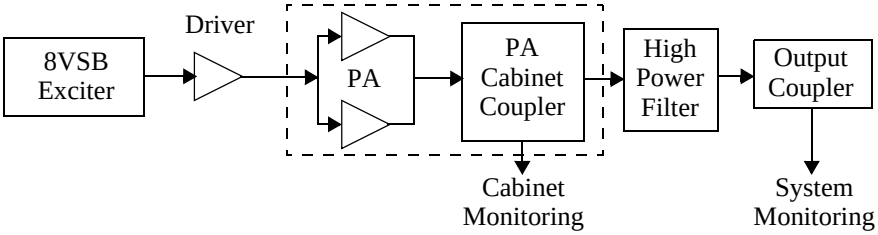
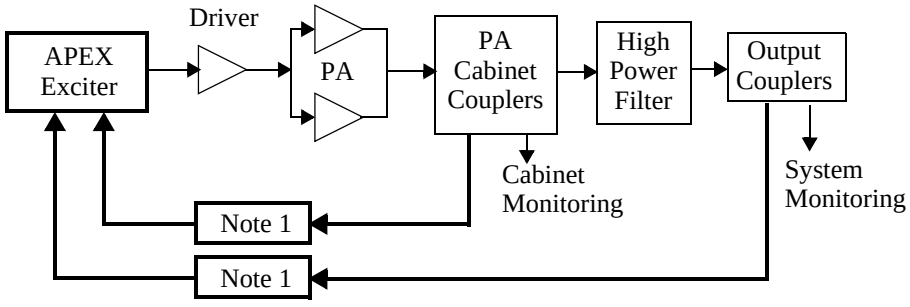


Figure 2-8 Diamond Transmitter with Single PA Cabinet



Note 1. These two boxes represent the 2-way splitters that are installed for feeding the RTAC samples to dual exciters. Terminate the unused outputs in 50 ohms.

Figure 2-9 Feedback Connections for Diamond Transmitter with Single PA Cabinet

WARNING: Disconnect primary power prior to servicing.

2.4.4.2 Diamond Transmitter - 1 PA Cabinet, 2 Exciters

If the Diamond transmitter system has dual exciters the feedback connections are modified by putting two-way, zero-phase splitters in each feedback sample line. The outputs of each splitter provide the appropriate feedback signal for each exciter, as shown in Figure 2-10.

If the cabinet and system monitoring outputs are not used, they should be terminated to prevent distortion of the APEX exciter feedback samples by the reflected signals.

The power level of each feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

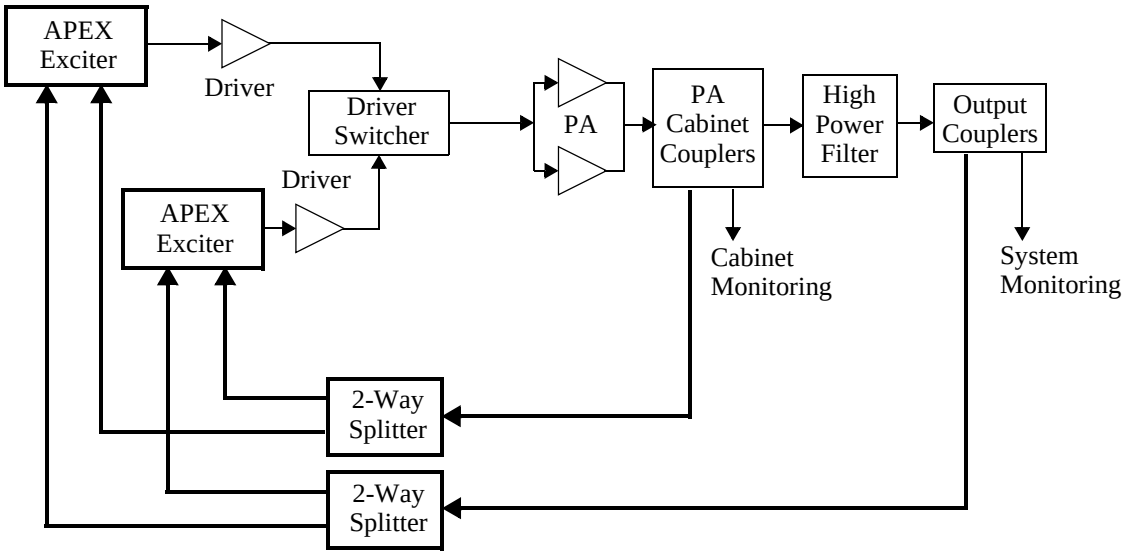


Figure 2-10 Diamond Transmitter - Single PA Cabinet - Dual APEX Exciters

2.4.4.3 Diamond Transmitter - 2 or More PA Cabinets

When the Diamond Transmitter has two or more PA cabinets, the feedback sample system has only one modification from the systems shown in Figure 2-10. The PA sample is still taken from the high power filter input coupler, but the cabinet combiner is now situated between the PA cabinet outputs and the high power filter input, see Figure 2-11.

If the transmitter system has dual exciters, as shown in Figure 2-12, feedback samples for each exciter are obtained by splitting each sample cable.

If the cabinet and system monitoring outputs are not used, they should be terminated to prevent distortion of the APEX exciter feedback samples by the reflected signals.

The power level of each feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

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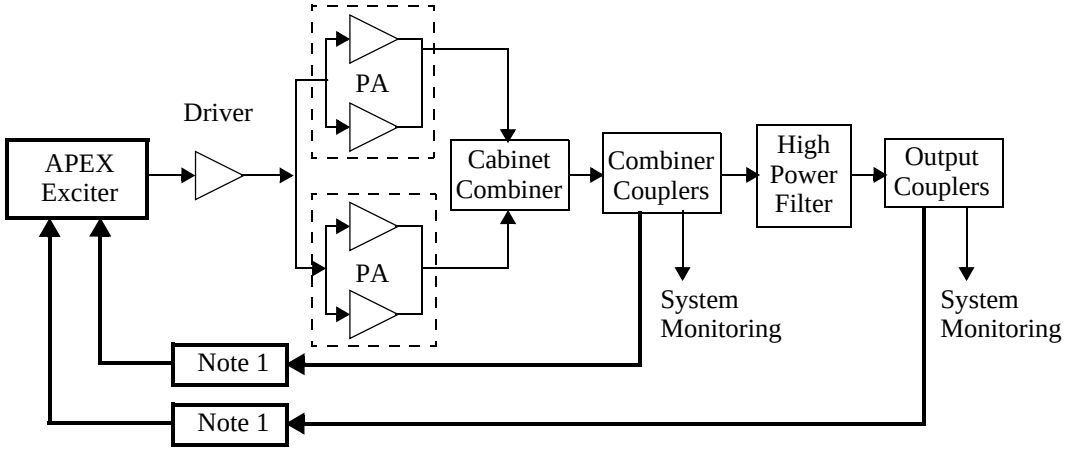


Note 1. These two boxes represent the 2-way splitters that are installed for feeding the RTAC samples to dual exciters. Terminate the unused outputs in 50 ohms.

Figure 2-11 Diamond Transmitter - Dual PA Cabinets - Single APEX Exciter

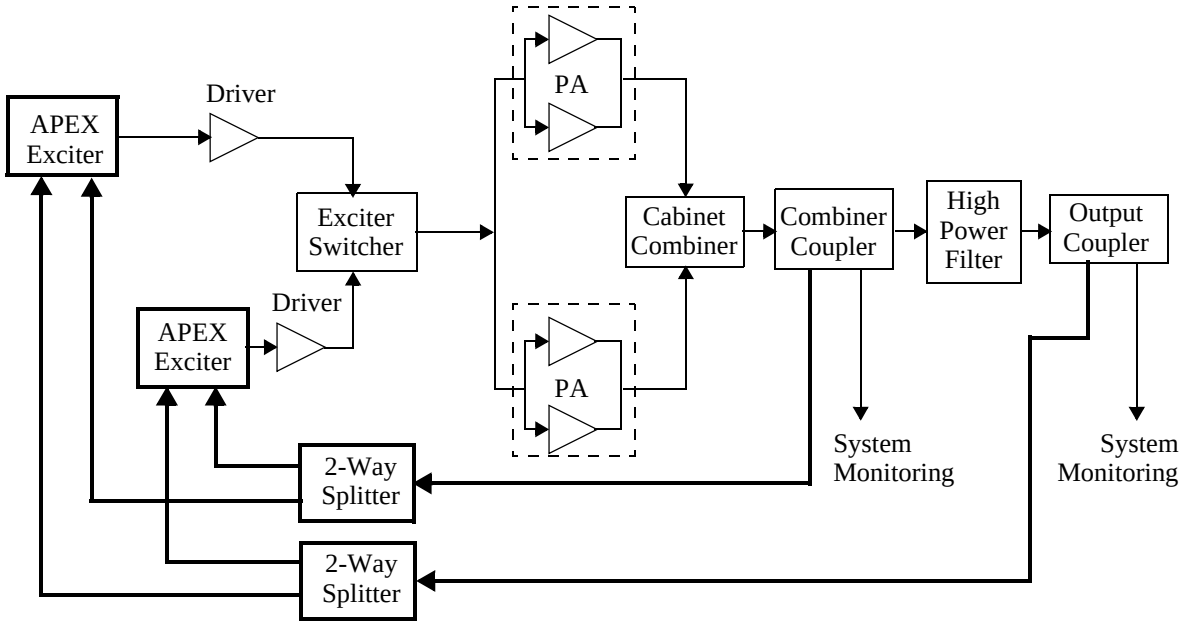


Figure 2-12 Diamond Transmitter - Dual PA Cabinets and APEX Exciters

WARNING: Disconnect primary power prior to servicing.

2.4.5 Sigma Transmitters

Sigma transmitters can be configured with one or more PA cabinets and single or dual exciters. Multiple PA cabinet systems can be configured with multiple high power filters. This gives rise to five feedback systems, as described below.

2.4.5.1 Sigma Transmitters - 1 PA Cabinet and Exciter

In the existing system, shown in Figure 2-13, the cabinet monitoring signals taken from the PA cabinet coupler and the high power filter output coupler. These signals are split with a directional couplers with the coupled outputs connected to the APEX exciter feedback input, as shown in Figure 2-14.

The power level of each feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

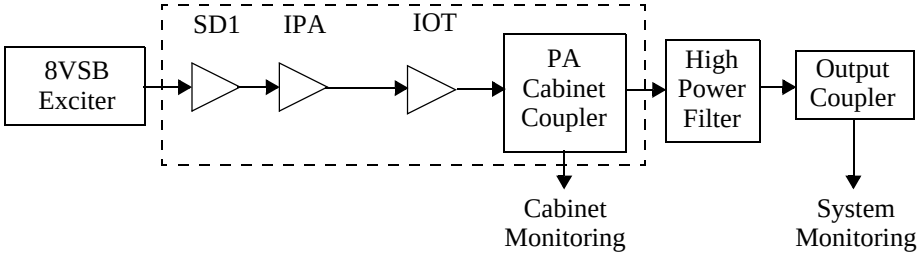
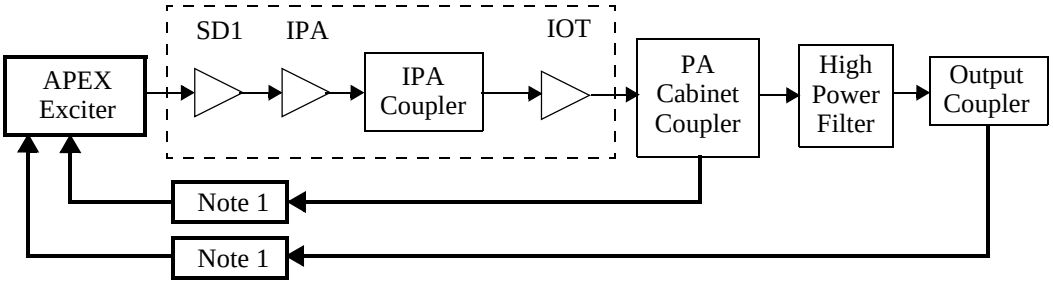


Figure 2-13 Sigma Transmitters - Single PA Cabinet and Exciter



Note 1. These two boxes represent the 2-way splitters that are installed for feeding the RTAC samples to dual exciters. Terminate the unused outputs in 50 ohms.

Figure 2-14 Sigma Transmitters - Single PA Cabinet and APEX Exciter

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2.4.5.2 Sigma Transmitter - 1 PA Cabinet - 2 Exciters

If the Sigma transmitter system has dual exciters the feedback connections are modified by putting two-way, zero phase splitters in each of the feedback sample line. The outputs of each splitter provide the appropriate feedback signal for each exciter, as shown in Figure 2-15.

The power level of each feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

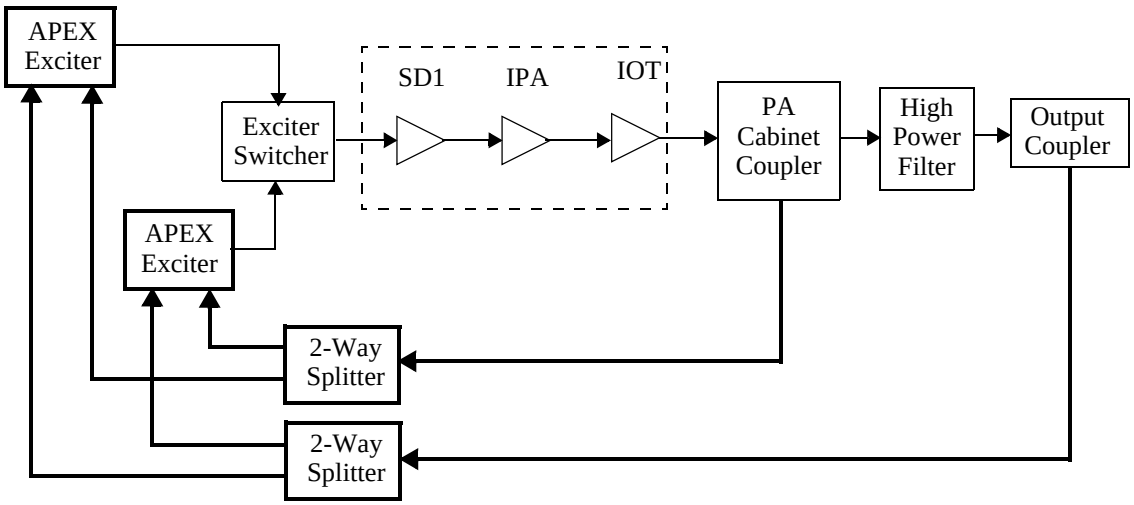


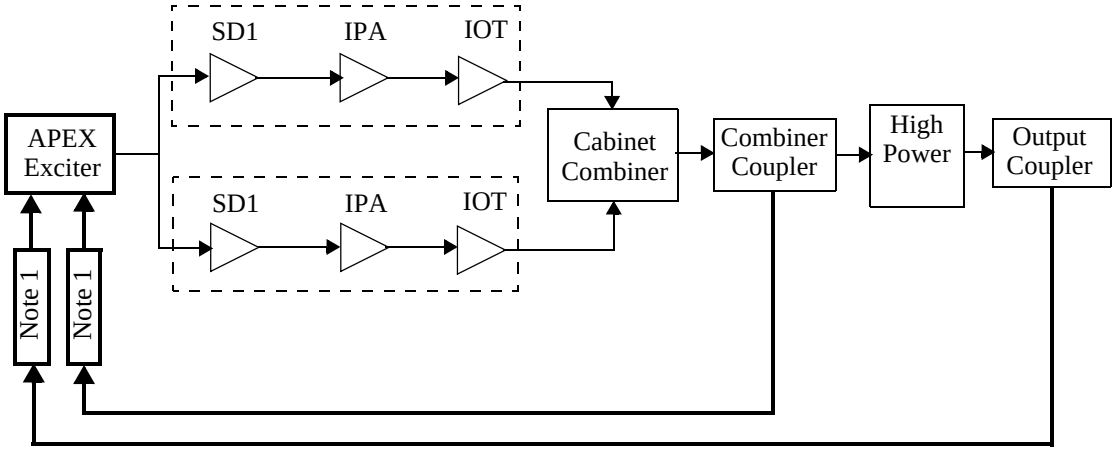
Figure 2-15 Sigma Transmitter - Single PA Cabinet - Dual APEX Exciters

WARNING: Disconnect primary power prior to servicing.

2.4.5.3 Sigma Transmitter - 2 or More PA cabinets

When the Sigma transmitter has two or more PA cabinets, the feedback signals are connected as shown in Figure 2-16.

- The HPF feedback sample is taken from the high power filter output coupler.
- The PA sample is taken from the cabinet combiner output coupler.
- If the transmitter system has dual exciters, feedback samples for each exciter are obtained by splitting each sample cable, as shown in Figure 2-17.
- If the transmitter system has one exciter, the splitters are still installed in the feedback samples, with the unused output port terminated into 50 ohms.
- The feedback signals at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The sample input power range is -10 to 0 dBm.



Note 1. These two boxes represent the 2-way splitters that are installed for feeding the RTAC samples to dual exciters. Terminate the unused outputs in 50 ohms.

Figure 2-16 Sigma Transmitter - Dual PA cabinets - Single APEX Exciter

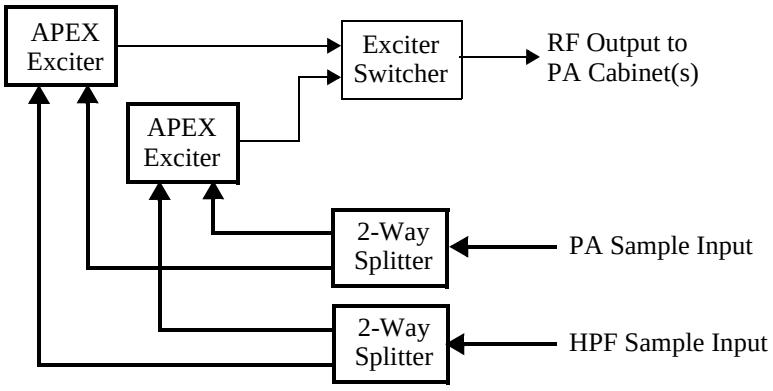


Figure 2-17 Sigma Transmitter - Showing Modifications for Dual APEX Exciters

WARNING: Disconnect primary power prior to servicing.

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2.5 Sigma Transmitter - 2 PA Cabinets, High Power Filters, and Exciters

When the Sigma transmitter has two or more PA cabinets and a high power filter for each PA cabinet the required feedback sample system is shown in Figure 2-18.

- The corresponding samples from the inputs of each filter are connected to a two-way combiners using equal lengths of cable. One of the two cables must include a phase shifter, which consists of a specific length of additional cable.
- A zero phase splitter, such as the two three, and four way units listed in Section 2.7 on page 2-17, is used to combine the samples.
- The lengths of the cables connecting the coupler to the inputs of the two-way combiner should be adjusted to equalize the phase of the PA samples, since the PAs may be operating in phase or out of phase by 90° increments.
- Before adjusting the phase shifter, all PA cabinets should be properly combined for minimum reject power.
- Proper adjustment of the phase shifter should yield maximum output power from the combiner, when measured with a spectrum analyzer, wattmeter, or millivolt meter. The phase of the two signals must be within 20°, this may necessitate a slight change of sample cable length to achieve. If the phase error is too large, the signals will cancel or develop a tilt or notch in the combined response.

The feedback signal at the exciter input should be padded to yield 0 dBm at the highest expected transmitter output power. The maximum input range is -10 to 0 dBm.

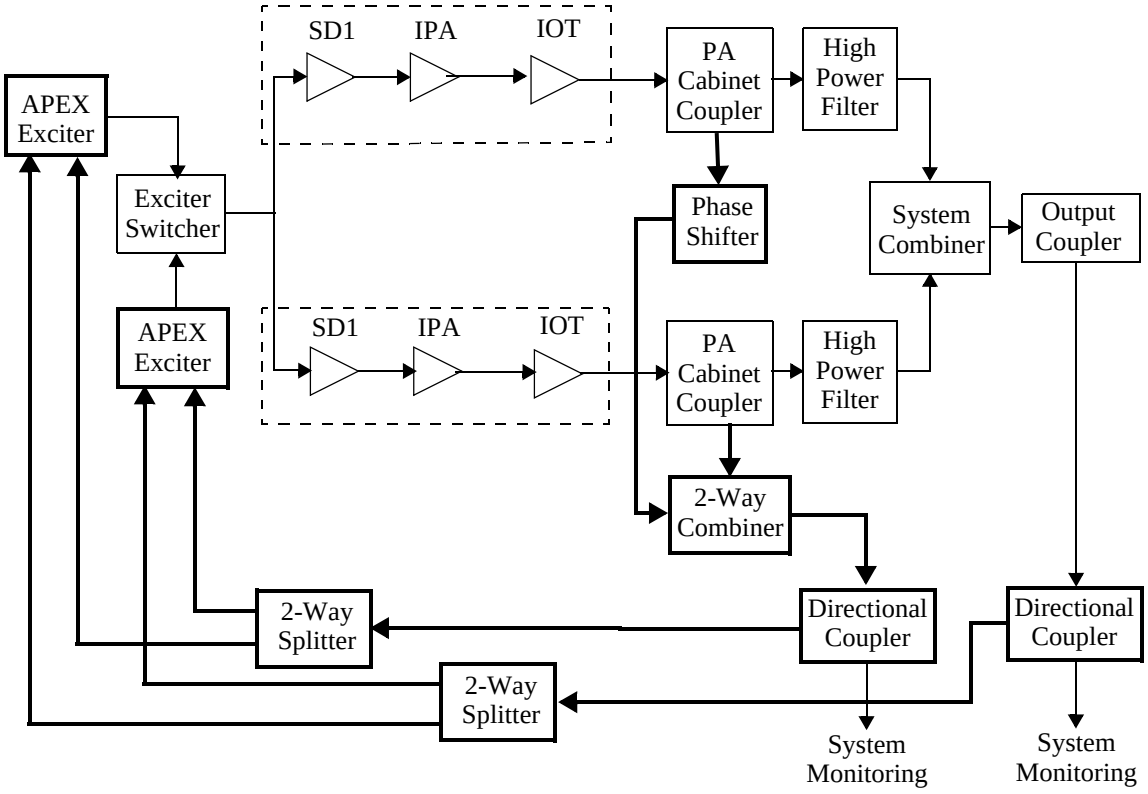

Figure 2-18 Sigma Transmitter - Dual PA Cabinets, High Power Filters, and APEX Exciters

WARNING: Disconnect primary power prior to servicing.

2.6 Configuring the Exciter

The APEX exciter is configured by the LCD touch screens. The basic functions of these screens are discussed in chapter 3 of this manual. It is necessary to be familiar with these screens in order to configure the exciter. This procedure is only a configuration checklist.

This procedure needs to be done in two parts.

- First it is necessary to get the exciter on channel and verify its operation on the bench.
- Next, after installation in the transmitter and connecting the feedback lines (which must be within the range of -10 to 0 dBm), the adaptive processor can be turned on and the transmitter performance can be checked.

Some transmitters may experience nuisance overdrive trips which are caused by the RTAC non-linear correction peak stretch capability. This can be prevented by programming the maximum peak stretch parameter of the RTAC setup screen, see Section 3.6.2.2, Max Peak Stretch, on page 3-33.

2.6.1 Configuration of Setup Screens

The initial part of exciter configuration involves portions of the following setup screens.

Main Screen.

- Set exciter RF output power (the display reads average power).
- Set the three RTAC functions. These refer to the three RF feedback signals which are connected to the rear panel of the exciter. These settings determine how the exciter will pre correct for the transmitter system linear and nonlinear distortions.

  Lin IPA: (linear intermediate power amplifier) is set to bypass, since the IPA Sample input on exciter rear panel is not used.

  Lin HPF: (linear high power filter), called HPF Sample on exciter rear panel.

  Non-Lin: (nonlinear input), called PA Sample on exciter rear panel.

Main Screen > Setup > Exciter Setup.

- Set the exciter to the correct channel.

  The channel box will be greyed out (and unattainable) if the diagnostic setup feature is locked. Instructions to lock or unlock the diagnostics setup is found in Section 3.6.6.2, Diagnostics Setup (Locked or Unlocked), on page 3-44.
- Enter any required pilot frequency offset.

  The pilot frequency offset box will be greyed out (and unattainable) if the diagnostic setup feature is locked. Instructions to lock or unlock the diagnostics setup is found in Section 3.6.6.2, Diagnostics Setup (Locked or Unlocked), on page 3-44.
- Select the transmitter type.
- Select the type and length (in feet) of waveguide, if waveguide is used in the system. The waveguide selections are listed below.
  - WR1800, rectangular, for channels 14 through 35
  - WR1500, rectangular, for channels 20 through 56
  - WR1150, rectangular, for channels 46 through 69
  - GLW1750, circular, for channels 14 through 19 and 24 through 41
  - GLW1700, circular, for channels 20 through 23

- GLW1500, circular, for channels 39 through 55.
- GLW1350, circular, for channels 56 through 69.

If the exciter is being bench tested, the waveguide selection can be set to None, to prevent group delay pre distortion of the RF output signal.

- Check the exciter RF output power calibration (the exciter display reads average power), if an accurate milliwatt meter is available. If necessary, perform a calibration. Power calibration is covered in Section 3.6.1.2 on page 3-31.

Main Screen > Setup > RTAC Setup.

- Max Peak Stretch can be used to avoid nuisance overdrive trips.
- RTAC Off-Air Mode is used to determine RTAC startup mode when the exciter (or transmitter) is off line.

Main Screen > Setup > Display Setup.

- Enter the Date and Time.
- Enter a new page title, if something other then APEX Exciter is desired.
- Chart selection allows the operator to view the Main screen response display at various points along the transmitter system.
- LCD Contrast allows operator to change contrast of the LCD display. Higher numbers produce greater contrast, lower numbers produce less contrast.

Main Screen > Setup > External I/O Setup.

This screen is used to set up the control/status jack on the rear of the exciter. This connector contains the provisions for external control and monitoring of the exciter.

When custom is selected in the transmitter selection section of the exciter setup screen, the channel functions (status and control) can be programmed.

- VSWR foldback low and high thresholds are programmable, see Section 3.6.4.1, VSWR Foldback Parameters, on page 3-35.
- Exciter switching threshold is determined by the power level of the on line exciter, see Section 3.6.4.2, RF Present Cutoff, on page 3-36.

Main Screen > Setup > Serial I/O Setup.

This screen is used to set up the front and rear panel RS-232 ports and the Ethernet port, marked LAN 10 Base-T on the exciter rear panel.

Main Screen > Setup > Change Password (or Security) Setup.

This screen provides a means of changing the user and diagnostics passwords. The existing passwords can be determined by entering either the User or Diagnostic Password choices.

The password becomes important if the User Setup or the Diagnostics Setup (or both) are to be locked.

Main Screen > Setup > User Setup (Lock or Unlock).

It is possible to lock the User Setup without a password, but the correct password is required to unlock it.

Main Screen > Setup > Diagnostic Setup (Lock or Unlock).

It is possible to lock the Diagnostic Setup without a password, but the correct password is required to unlock it.

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2.6.2 Configuration of Status Screens

When configuring an exciter for the first time, it is useful to check certain portions of the following status screens.

Main Screen > Status > MPEG Input.

- This screen should show no faults if the MPEG-2 SMPTE 310M transport stream is present at the exciter input.

  If the transport stream is missing the Signal Strength will show 0%, and the 43 MHz (VCO) Control, SMPTE Input, and SMPTE Output will all show fault.

Main Screen > Status > Adaptive Processing.

- IPA Feedback (IPA feedback signal), HPF feedback (RF sample from output of high power filter), and Amp Feedback (RF power amplifier output sample) bargraphs:

  The HPF and Amp bargraphs, each of which contain blue (peak power) and yellow (average power) traces, should be within their active travel ranges if the feedback signals are within the correct power range (-10 to 0 dBm), the IPA bargraph will show zero, since it is not used.

  If the signal is out of range, that input will fault.

- ADC OvrRange (analog to digital converter over range) will be Ok if all feedback signals are within their proper ranges, and will fault if any are too large.

Main Screen > Status > Digital Processing.

- MPEG Sync and MPEG Valid will both fault if the MPEG transport stream is missing from the exciter.

Refer to chapter 3 in this manual if the rest of the status screens are to be checked.

2.6.3 Normal Settings for Diagnostic Screens

The Diagnostics screens offer tests used to diagnose exciter problems. If the diagnostic selections are left in the wrong states, normal operation of the exciter could be impaired. The default values for the diagnostics screens can be found in Table 5-1 on page 12.

The following is a list of the normal states of the diagnostic functions and the exciter mute.

Status > Adaptive Processing > Diagnostics

- LoopBack: None
- Test Tones: Disabled

Status > Digital Processing > Modulator Board > Diagnostics

- Nyquist Filter Data: Enabled
- Nyquist Test Pattern: Disabled

Status > IF & RF Processing > Down Converter > Diagnostics

- RF Sample Select: Automatic
- RF Sample AGC: Enabled

Status > System Control > External I/O Board > Diagnostics

- Analog Loopback: Disabled

Setup >Exciter > Exciter Setup screen> Mute soft key.

- The exciter is normally un-muted. Pressing the button will open a sub window which will have instruction to mute or un-mute the exciter output.

2.7 Materials Needed

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The following list represents the materials that may be used for the various field installs. Not all materials are required for every installation.

- Coupler, Mini Circuit, ZFDC-10-21, 50 ohm BNC, Harris part number 620-2969-000

  This coupler is used when a spare sample is not available. It is place in line at the measurement point and the coupled port used for the feedback.
  The coupled port has a 10 dB attenuation from the input.

- Splitter, two port, Mini Circuits, ZFSC-2-2, zero phase, 50 ohm SMA, Harris part number 620-2964-000

  This splitter is used to split the feed back signals to two exciters.

- Splitter, two port, Mini Circuits, ZFSC-2-2, zero phase, 50 ohm BNC, Harris part number 620-1563-000

  This splitter is used to combine the PA feed back signal from two PA cabinets if separate mask filters are used for each PA.

- Splitter, four port, Mini Circuits, ZFSC-4-1, zero phase, 50 ohm BNC, Harris part number 620-2833-000

  This splitter is used to combine the PA feed back signal from three or four PA cabinets if separate mask filters are used for each PA. For combining samples from three PA cabinets, terminate unused input port.

- Adapters, N female to BNC male, Harris part number 620-0128-000

  Used to connect a BNC coupler directly to the N connector on the RF system.

- Adapter, BNC female to N male, Harris part number 620-0547-000

  Used to connect the original RF system cable to feedback coupler.

- Adapter, BNC male to BNC male, Harris part number 620-0564-000

  Used in Platinum transmitters to connect the feedback coupler directly to the RF sample coupler.

- Adapter TNC female to BNC male, Harris part number 620-2967-000

  Used in Sigma to connect the feedback coupler directly to the breakaway couplers.

- Adapter, BNC female to TNC male, Harris part number 620-2821-000

  Used in Sigma to connect original breakaway coupler cable to the feedback coupler.

- RF Cables, the number and type of each depends on transmitter type and installation. Depending on installation, other lengths and connector combinations may be needed.

  30 ft, RG223, 50 ohm, BNC male to SMA male

  30 ft, RG223, 50 ohm, BNC male to BNC male

  30 ft, RG223, 50 ohm, N male to BNC male

  30 ft, RG223, 50 ohm, N male to SMA male

  30 ft, RG223, 50 ohm, N male to N male

  10 ft, RG223, 50 ohm, BNC male to SMA male

  3 ft, RG223, 50 ohm BNC to BNC

  3 ft, RG223, 50 ohm BNC to SMA male

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3 Operating the APEX Exciter

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Operating the APEX exciter requires knowledge of two sets of controls.

First is the power off/on switch, which is not normally used if the exciter is mounted in a transmitter, but could be used if the exciter is used as a signal source apart from a transmitter. The power off/on switch is located on the right side of the exciter rear panel when facing the rear of the exciter.

The most important part of exciter operation is knowledge of the LCD display touch screens, which is covered in the remainder of this chapter.

3.1 Basic Operating Procedure

After the exciter has been installed and set up, the two most often used operating functions are raising or lowering the exciter RF output power and locating exciter faults if a malfunction should occur. These two topics will be addressed before the subject of the LCD screen navigation is covered.

3.1.1 Raising or Lowering Output Power

The average output power of the exciter in mW is displayed on the Main screen. Exciter output power adjustment soft keys are also included on the Main screen, and appear as arrows to the left and right of the output power display.

On the Main screen, output power can also be set by touching the numbers in the power display. This brings up a number pad where a new value for output power (between 0 and 250 mW average power) can be entered. When new value is entered, it is accepted by touching Done or the old power retained by pressing Cancel.

Exciter power raise and lower can also be controlled remotely. In most transmitters, exciter power is controlled from the transmitter, with transmitter output power controlled locally and remotely by a separate circuit. In some transmitters the exciter output power control is the transmitter output power control, and is available by remote control.

3.1.2 Exciter Fault Display - Red

The exciter includes several LCD status screens which display normal or fault operating conditions. If a fault occurs within the exciter, a red FAULT button appears at the bottom of each screen. Touching the fault button switches to the System Status screen, which will display a FAULT status beside the offending section of the exciter. Touching the faulted box causes the status display for that box to appear. This display gives additional information concerning the problem within that section and will point to a circuit board and/or a signal condition.

3.1.2.1 Fault Warning - Yellow

When status screen parameters approach their limit, a yellow warning will replace the Green OK indication at the bottom of the screens.

When VSWR foldback is active the system control light on the front panel will be lighted yellow.

3.2 Starting Point: The Main LCD Touch Screen

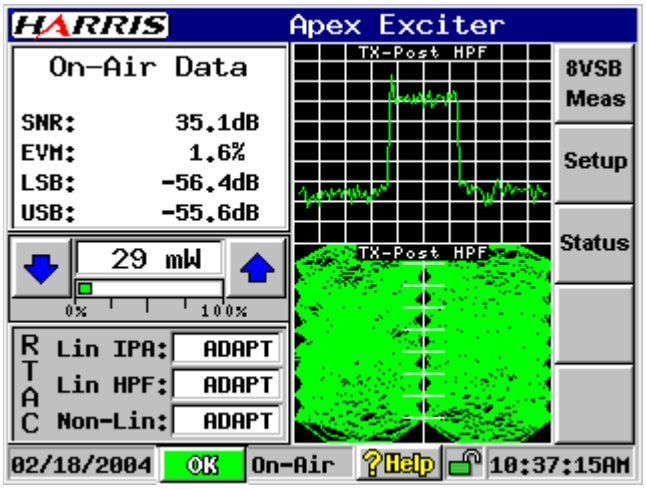

Figure 3-1 LCD Main Screen

Setup, operation, and trouble shooting of the APEX exciter is accomplished via the LCD Display Touch Screens. This chapter covers the use and definitions of the screens.

When power is first applied, a power up screen appears briefly, but the display quickly changes to the main screen, shown in Figure 3-1.

The **main screen** is divided into several areas, these are as follows.

- On-Air Data block shows:

  Signal to noise ratio (SNR)

  Error vector magnitude (EVM)

  Integrated power of the lower sideband (LSB) and upper sideband (USB) over the spectrum of the lower and upper adjacent channels with reference to the RF output of the high power filter.
- Exciter output power control and level display.
- RTAC section of the main screen shows the operating status of its three correctors, which are:
    - Lin IPA (IPA RF feedback sample)
    - Lin HPF (RF feedback sample taken after the high power filter)
    - Non-Lin (PA output feedback sample, taken before the high power filter).

  The possible states for each corrector are:
    - Bypass: Turns the selected corrector off
    - Default: Selects a pre loaded correction algorithm from the RTAC Filter Set-up screen. Saving an RTAC correction algorithm to an RTAC filter is covered in Section 3.6.2 on page 3-32.
    - Adapt: Turns the selected corrector on

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- Hold: Keeps the last correction value for the selected mode. This is a short term option. For long term use select Default.

- RF spectrum display at selected locations throughout the transmitter RF system.
- Eye pattern: a fixed display for the output of the high power filter (HPF).

  If the Main screen - RTAC - Lin HPF is set to Adapt, Hold, or Default and an RF feedback is applied to the HPF input or the Status >Adaptive Processing Status > Diagnostics screen loopback function is set to Digital, an eye pattern will be displayed. If the loopback function is set to analog, the RTAC Lin HPF must be set to Adapt to get an eye pattern.

  If the Main screen - RTAC - Lin HPF is set to Bypass, the eye pattern will show noise. It will also show noise if Lin HPF is set to Adapt, Hold, or Default and no RF feedback is applied to the HPF input and the Status >Adaptive Processing Status > Diagnostics screen loopback function is set to none. The loopback function is covered in Section 3.4.3.1 on page 3-12.

  If waveguide group delay precorrection is active, this precorrection will be subtracted out of the exciter eye display.

Several Main Screen soft keys are provided to start the process of navigation through the various LCD screens. These areas include 8VSB Meas (measure), Status, Setup, or Fault.

Another Main Screen option at the top of the screen is the 8VSB Meas (measure) soft key. Pressing this key provides access to three screens which furnish information concerning the transmitter distortions and exciter corrections.

3.2.1 Spectrum Response and Eye Pattern Screen

If the RF spectrum or eye pattern areas of the main screen is touched, a full screen display of that selection is presented. The spectral response can be displayed at several locations through out the transmitter RF system. Locations for this display include:

- 8VSB w/RTAC: Digital signal taken at output of adaptive precorrector board.
- 8VSB Ref: Digital signal obtained at the output of the modulator board.
- BIT: Digital signal obtained at modulator to adaptive precorrector board interface.
- Exciter: RF signal is taken from J4 sample output of exciter PA and connected to J4 sample input on down converter board.
- IPA: From rear panel RF sample input labeled IPA Sample.
- Tx-Pre HPF: From rear panel RF sample input labeled PA Sample.
- Tx-Post HPF: From rear panel RF sample input labeled HPF Sample.

The location for the eye pattern display is fixed at the output of the high power filter (HPF).

If the Main screen - RTAC - Lin HPF is set to Adapt, Hold, or Default and an RF feedback is applied to the HPF input or the Status >Adaptive Processing Status > Diagnostics screen loopback function is set to Digital, an eye pattern will be displayed. If the loopback function is set to analog, the RTAC Lin HPF must be set to Adapt to get an eye pattern.

If the Main screen - RTAC - Lin HPF is set to Bypass, the eye pattern will show noise. It will also show noise if Lin HPF is set to Adapt, Hold, or Default and no RF feedback is applied to the HPF input and the Status >Adaptive Processing Status > Diagnostics screen loopback function is set to none. The loopback function is covered in Section 3.4.3.1 on page 3-12.

WARNING: Disconnect primary power prior to servicing.

3.2.2 Exciter Status Series of Screens

Selecting the main screen Status button accesses the Exciter Status screen.

Five smaller boxes are displayed within the System Status screen. These boxes represent circuit functions within the exciter. Touching any of the five boxes brings up the status sub screen (or screens) for that circuit board. Within any of these screens, touching Home returns to the main screen, and touching Status or Fault brings up the System Status screen. Pictures and descriptions of these screens are found in Section 3.4 on page 3-8.

3.2.3 Exciter Setup Series of Screens

Selecting the Main screen Setup button accesses the System Setup screen. Nine smaller boxes are displayed within the System Setup screen. These boxes represent programmable areas within the exciter. Touching any of the nine boxes brings up the setup sub screen for that area. Within any of these screens, touching Home returns to the main screen, touching back returns to the System Setup screen, and touching Fault (at the bottom of the screen, if a fault exists) brings up the System Status screen. Pictures and descriptions of these screens are found in Section 3.6 on page 3-27.

3.2.4 8VSB Measure Soft Key

The 8VSB Meas (measure) soft key at the top of the main screen provides information concerning the transmitter system distortions and exciter corrections for them. This information is given in three screens. They are:

- Transmitter/Systems Linearity screen. This screen refers to the amplifier caused non-linear distortions, which are linearity (called amplitude on the screen) and phase distortion (called phase on the screen).
- Amplitude and Phase Correction screen. This screen refers to the exciter corrections for the amplifier caused non-linear distortions, which are linearity (called amplitude on the screen) and phase distortion (called phase on the screen).
- Amplitude and Group Delay Correction screen. This screen refers to the linear distortions caused by the filters, tuned circuits, and other amplitude response shaping circuits in the transmitter system. These distortions are frequency response errors (called amplitude on the screen) and group delay.

3.3 LCD Display Flow Chart

Refer to Figures 3-2 to 3-4. Navigation is started from the main screen by lightly touching Status, Setup, Fault, the spectrum display, or the Eye Pattern display.

- From any screen, other than the main screen, Home returns to the main screen.
- From any screen, Fault brings up the System Status screen.
- From any sub screen within setup, pressing Back returns to the System Setup screen.
- From any sub screen within status, pressing Status returns to System Status screen,
- Some System Status sub sections are composed of several (two to four) sub screens. Within these sections, Next and Prev (previous) sequentially walks through the sub screen selections.
- Some status sub screens include a diagnostic screen. This screen provides additional information for the screen in question.

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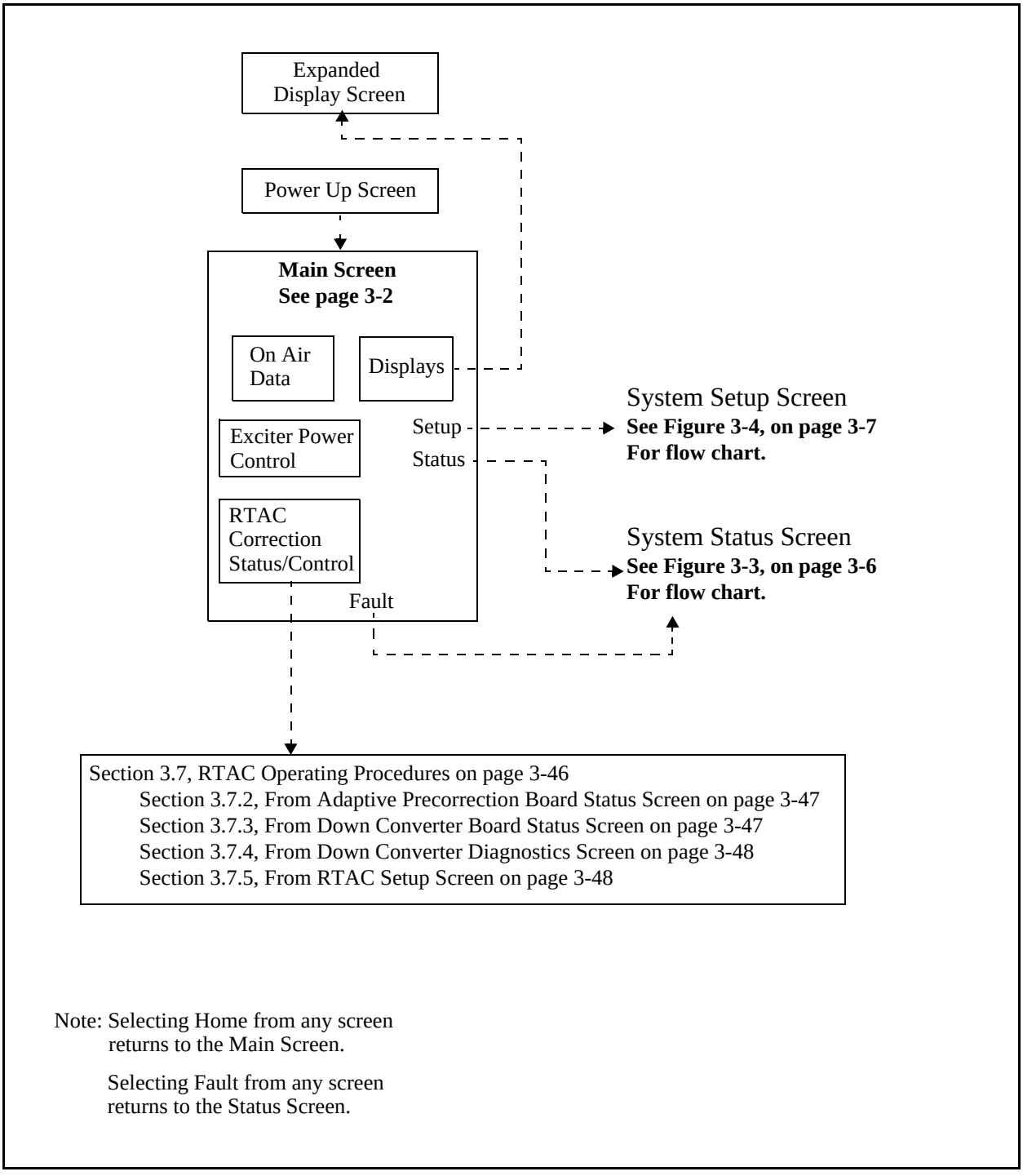
Expanded Display Screen
Power Up Screen
Main Screen
See page 3-2
On Air Data
Displays
Exciter Power Control
RTAC Correction Status/Control
Setup
Status
Fault
System Setup Screen
See Figure 3-4, on page 3-7
For flow chart.
System Status Screen
See Figure 3-3, on page 3-6
For flow chart.
Section 3.7, RTAC Operating Procedures on page 3-46
Section 3.7.2, From Adaptive Precorrection Board Status Screen on page 3-47
Section 3.7.3, From Down Converter Board Status Screen on page 3-47
Section 3.7.4, From Down Converter Diagnostics Screen on page 3-48
Section 3.7.5, From RTAC Setup Screen on page 3-48
Note: Selecting Home from any screen returns to the Main Screen.
Selecting Fault from any screen returns to the Status Screen.

Figure 3-2 Main Screen, APEX Exciter LCD Display Flow Chart

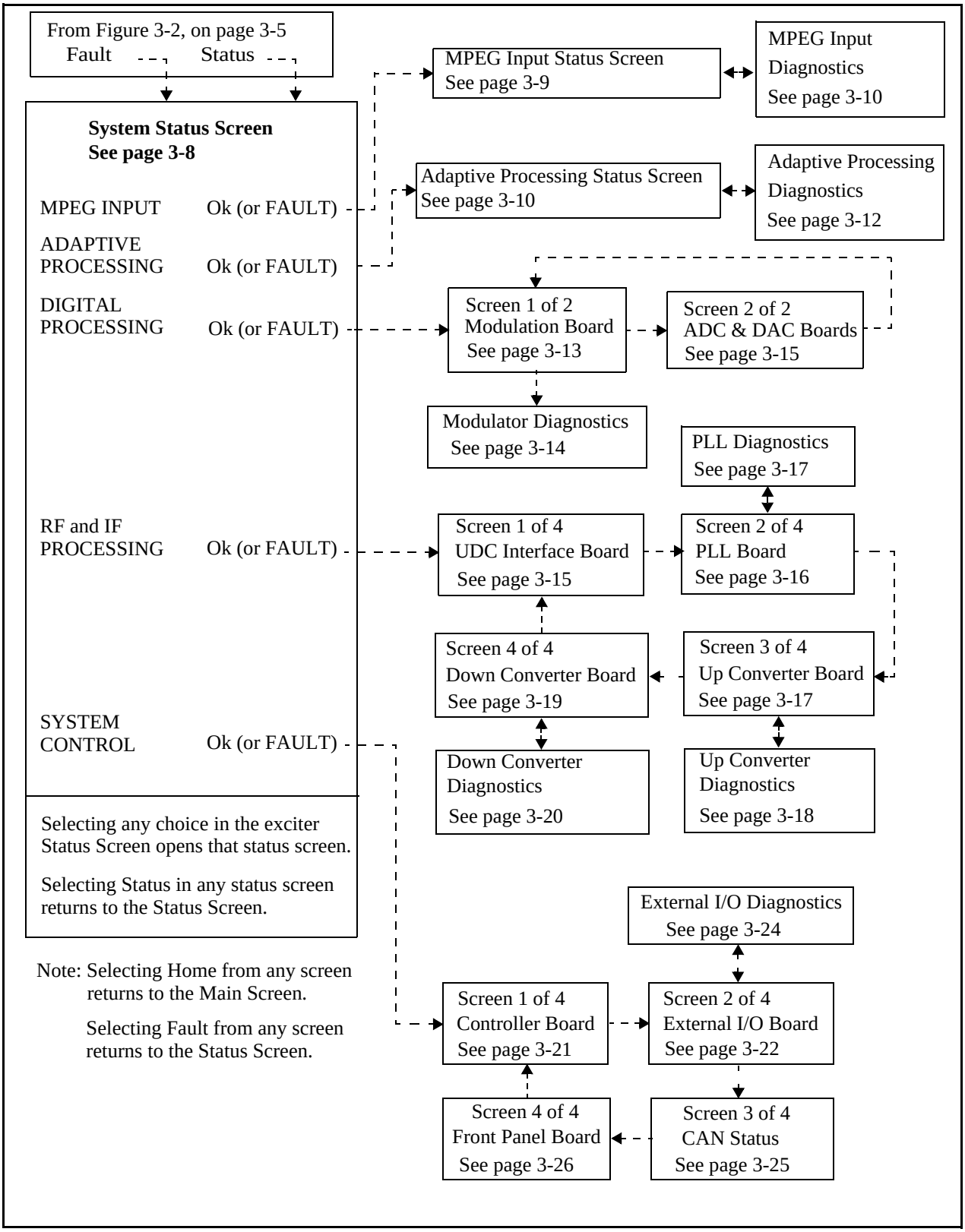
From Figure 3-2, on page 3-5
Fault
Status
System Status Screen
See page 3-8
MPEG INPUT Ok (or FAULT)
ADAPTIVE PROCESSING Ok (or FAULT)
DIGITAL PROCESSING Ok (or FAULT)
RF and IF PROCESSING Ok (or FAULT)
SYSTEM CONTROL Ok (or FAULT)
Selecting any choice in the exciter Status Screen opens that status screen.
Selecting Status in any status screen returns to the Status Screen.
Note: Selecting Home from any screen returns to the Main Screen.
Selecting Fault from any screen returns to the Status Screen.
MPEG Input Status Screen
See page 3-9
MPEG Input Diagnostics
See page 3-10
Adaptive Processing Status Screen
See page 3-10
Adaptive Processing Diagnostics
See page 3-12
Screen 1 of 2 Modulation Board
See page 3-13
Screen 2 of 2 ADC & DAC Boards
See page 3-15
Modulator Diagnostics
See page 3-14
PLL Diagnostics
See page 3-17
Screen 1 of 4 UDC Interface Board
See page 3-15
Screen 2 of 4 PLL Board
See page 3-16
Screen 4 of 4 Down Converter Board
See page 3-19
Screen 3 of 4 Up Converter Board
See page 3-17
Down Converter Diagnostics
See page 3-20
Up Converter Diagnostics
See page 3-18
External I/O Diagnostics
See page 3-24
Screen 1 of 4 Controller Board
See page 3-21
Screen 2 of 4 External I/O Board
See page 3-22
Screen 4 of 4 Front Panel Board
See page 3-26
Screen 3 of 4 CAN Status
See page 3-25

Figure 3-3 Status Screens, APEX Exciter LCD Display Flow Chart

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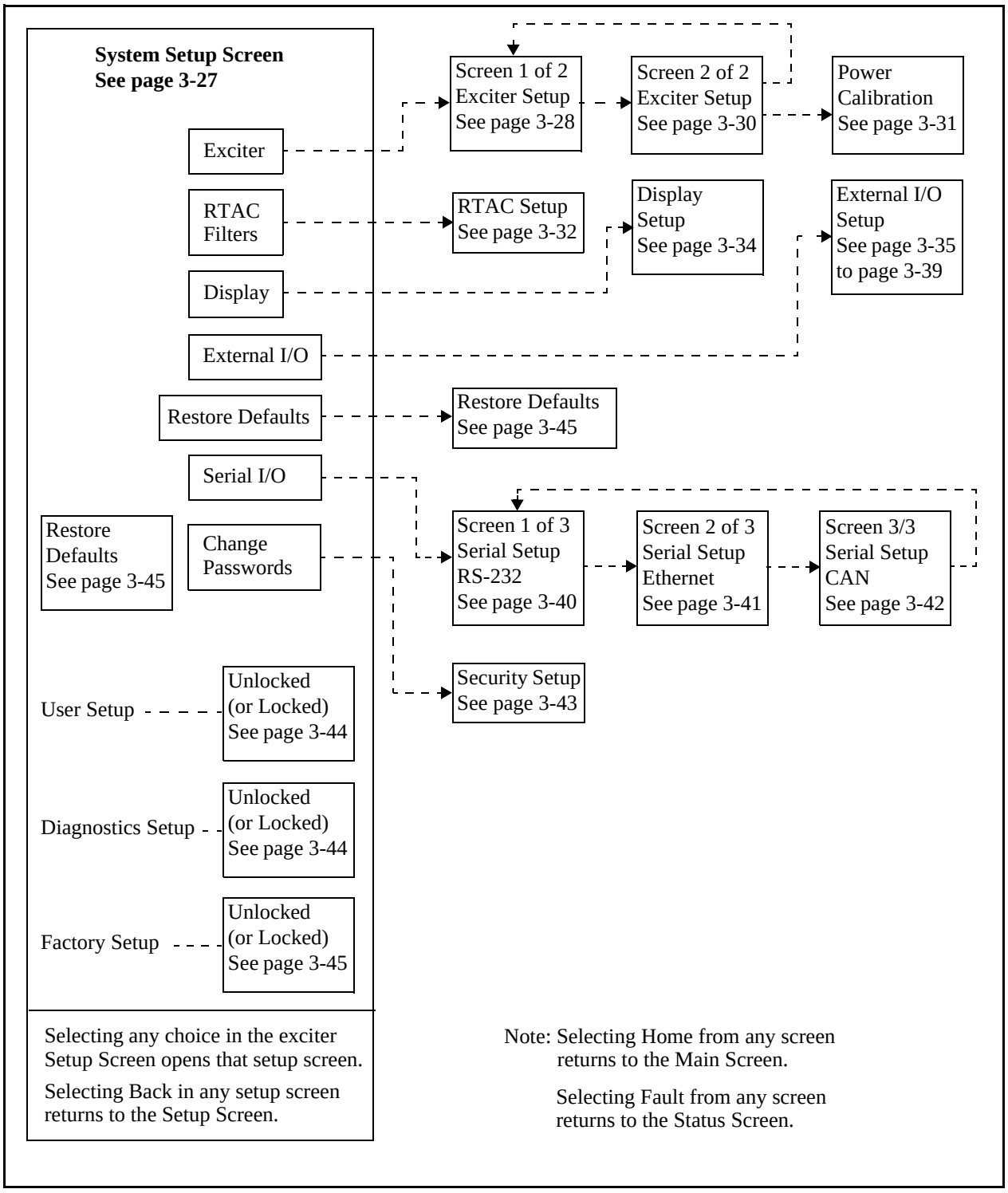
System Setup Screen
See page 3-27
Exciter
RTAC Filters
Display
External I/O
Restore Defaults
Serial I/O
Restore Defaults See page 3-45
Change Passwords
User Setup
Diagnostics Setup
Factory Setup
Unlocked (or Locked) See page 3-44
Unlocked (or Locked) See page 3-44
Unlocked (or Locked) See page 3-45
Screen 1 of 2 Exciter Setup See page 3-28
Screen 2 of 2 Exciter Setup See page 3-30
Power Calibration See page 3-31
RTAC Setup See page 3-32
Display Setup See page 3-34
External I/O Setup See page 3-35 to page 3-39
Restore Defaults See page 3-45
Screen 1 of 3 Serial Setup RS-232 See page 3-40
Screen 2 of 3 Serial Setup Ethernet See page 3-41
Screen 3/3 Serial Setup CAN See page 3-42
Security Setup See page 3-43
Selecting any choice in the exciter Setup Screen opens that setup screen.
Selecting Back in any setup screen returns to the Setup Screen.
Note: Selecting Home from any screen returns to the Main Screen.
Selecting Fault from any screen returns to the Status Screen.

Figure 3-4 Setup Screens, APEX Exciter LCD Display Flow Chart

WARNING: Disconnect primary power prior to servicing.

3.4 Details of the Exciter Status Screens

This section provides pictures and details of the Exciter Status screen, shown in Figure 3-5, and its sub screens. The sub screens give the status of selected control areas or PC boards.

If the Diagnostics Setup on the Exciter System Setup screen is locked, all diagnostics functions and the Exciter Setup screen Channel and Frequency Offset functions will be locked, and their various screen selection values will be greyed out.

3.4.1 System Status Screen

Refer to Figure 3-5. The System Status screen serves two purposes. First, it provides a general status of five items, and secondly it provides access to eleven sub screens which give additional status information about selected circuit boards within the exciter.

Five small boxes are displayed within the System Status screen. These boxes represent circuit boards or control areas within the exciter, see names in Table 3-1. The general status of each section (OK or FAULT) is displayed to the right of each box. Touching any of the boxes brings up the status screen for that selection.

Five hardware switches on the exciter front panel (to the immediate right of the LCD display) provide short cuts which leads directly to the five status areas listed in Table 3-1.

Table 3-1 System Status Screen Circuit Board Names

Box Name	Circuit Board Name
MPEG Input	SMPTE 310M Interface board, see page 3-9
Adaptive Processing	Adaptive Precorrector board, see page 3-10
Digital Processing (shown in two screens)	Modulator on page 3-13, and ADC and DAC boards page 3-15
IF and RF Processing (shown in four screens)	UDC Interface on page 3-15, PLL on page 3-16, Up Converter on page 3-17 and Down Converter on page 3-19
System Control (shown in four screens)	Controller board on page 3-21, External I/O board on page 3-22, CAN Bus on page 3-25, and Front Panel Board Status page 3-26
BIT (built in tests)	Built In Tests on page 3-26

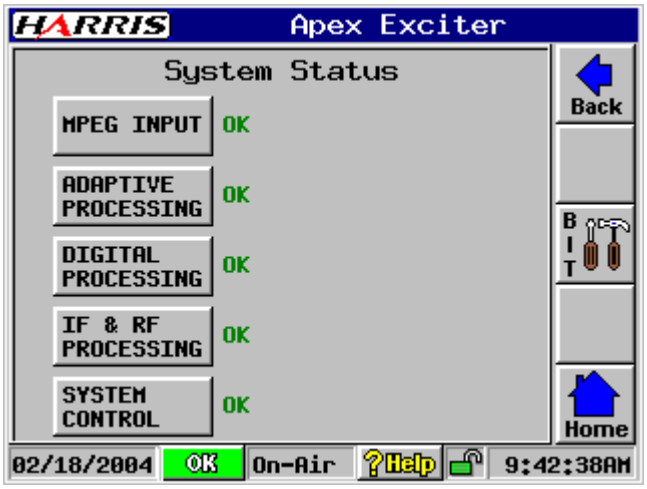

Figure 3-5 System Status Screen

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3.4.2 MPEG Input Status Screen

The MPEG Input Status screen is shown in Figure 3-6, with screen entries listed below.

- 3.3 Vdc: SMPTE 310 board receives 3.3 VDC from the modulator board.
- 5 Vdc: SMPTE 310 board receives 5 VDC from the modulator board.
- 43 MHz control: Control voltage to U15, the 43.048 MHz clock oscillator. Typical range = 2.23 to 2.34 volts, with 2.28 volts being nominal. This reading is affected by changing the MPEG Input Status > Diagnostics EEPot setting.

  This refers to the phase lock loop that locks the internal 43 MHz clock to the incoming SMPTE 310M transport stream clock.
- Signal Strength: Signal strength of the SMPTE 310 input signal. Typical range = 0% to 100%.
- EEPROM: (Ok or FAULT) The EEPROM is the local board memory. It stores board specific information such as board revision, CPLD revision, and other local data.
- SMPTE Input Lock: (OK or FAULT) Fault means no SMPTE 310M, 8VSB transport stream is present at the input. OK means SMPTE 310M input is valid.

  This input will show fault with a valid SMPTE 310M input to the exciter if the SMPTE test pattern selection of the exciter setup screen is set to anything but off.
- SMPTE Output Lock: (OK or FAULT) OK = output of SMPTE board is locked to a valid SMPTE 310M input. IF SMPTE 310M signal is not present, it will fault.

  A valid SMPTE 310 transport stream can be generated internally by selecting one of the test patterns in the SMPTE Test Pattern selection of the Exciter Setup screen.

  If a test pattern is selected, but no valid SMPTE 310M signal is present at the exciter input, the SMPTE Input Lock will still show fault but the SMPTE Output Lock and the Modulator board (located under Digital Processing Status) should show no faults.
- Board Rev: Revision level of the SMPTE 310M Interface board.
- CPLD Rev: Revision level of the CPLD in the SMPTE 310M Interface board.

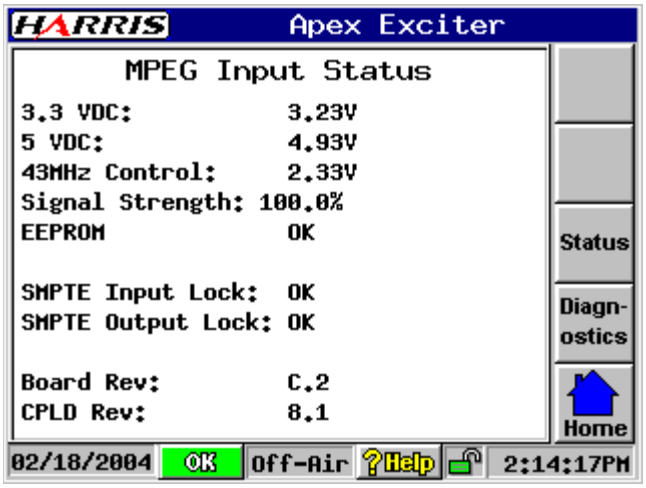

Figure 3-6 MPEG Input Status Screen

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3.4.2.1 MPEG Input Diagnostics

Refer to Figure 3-7. This screen capture represents the normal mode settings for the MPEG Input Diagnostics function. Screen entries are listed below.

- EE Pot: Number from 0 to 1023 entered via touch screen key pad to compensate for aging of 43 MHz crystal. The default value for this number is 0. If this setting is changed, the new value will remain after an AC power loss.

  Changing this setting causes the MPEG Input Status 43MHz Control voltage to change. Higher numbers cause frequency to go higher.

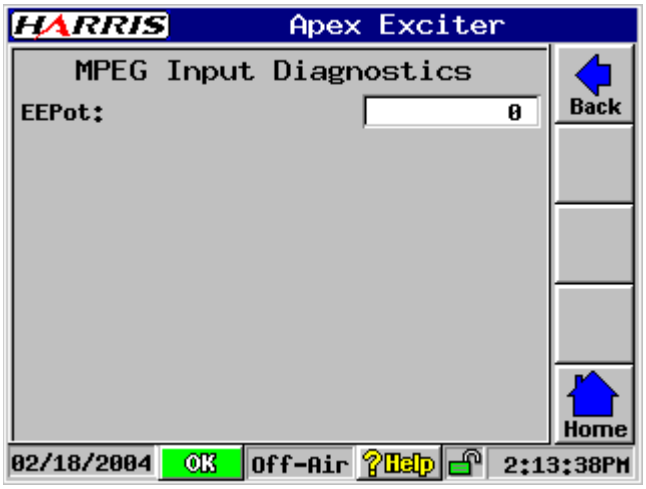

Figure 3-7 MPEG Input Diagnostics

3.4.3 Adaptive Processing Board Status Screen

The Adaptive Processing Board status screen is shown in Figure 3-8, with screen entries listed below.

- 3.3 Vdc: This is the output of the 3.3 V dc to dc converter.
- 5 Vdc: This is the board input voltage, which comes from the controller board.
- AP 3.3 Vdc supply is derived from the 3.3 Vdc supply through an FET switch. This voltage is switched off if the 1.9 Vdc AP supply faults.
- AP 1.9 Vdc: This is the output from the AP DSP core supply dc to dc converter.
- NL 3.3 Vdc supply is derived from the 3.3 Vdc supply through an FET switch. This voltage is switched off if the 1.8 Vdc NL supply faults.
- NL 1.8 Vdc NL DSP core power supply.
- PLL Lock: (Ok or FAULT) This is the lock status of a PLL on the adaptive corrector board. It locks the 10.762, 21.52, 43, and 86 MHz clocks to the 43 MHz clock from the SMPTE board.
- EEPROM: (Ok or FAULT) The EEPROM is the local board memory. It stores board specific information such as board revision, AP CPLD revision, DSP revision, and other local data.
- ADC Over Range: (OK or FAULT) Fault = One or more input RF voltage samples to the ADC (analog to digital converter) exceeded maximum allowable level.

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Each of the three feedbacks below has a bar graph. The yellow (upper) bar indicates average power level and the blue (lower) bar indicates peak level. The presence of an RF sample which is within the correct power range (-10 to 0 dBm) is indicated when both bars are within the center range of the window. The bar graphs are not calibrated to the input power level. If any input sample is outside the allowable power range window, the bars for that input will be at an extreme end of the window and that input will be faulted.

- IPA Feedback: (OK or FAULT)

  This is the RF sample taken before the power amplifier. It is normally not connected.

- HPF Feedback: (OK or FAULT)

  This is the RF sample taken after the high power filter.

- PA feedback: (OK or FAULT)

  This is the RF sample taken after the power amplifier but before the high power filter.

Note

The maximum input level for the three feedbacks mentioned above should not exceed +5 dBm. Excessive input levels will cause faults for the ADC and feedback inputs and can also cause crosstalk between inputs and/or damage to the exciter. +20 dBm is the damage level

- NL CPLD: (Ok or FAULT) This is the health status of the NL CPLD in the Adaptive Precorrector board.
- Board Rev: This is the board revision for the Adaptive Precorrector board.
- AP CPLD Rev: This is the revision level of the AP CPLD in the Adaptive Precorrector board.
- AP DSP Rev: This is the revision level of the AP DSP (digital signal processor) software in the Adaptive Precorrector board.
- NL DSP Rev: This is the revision level of the NL DSP (digital signal processor) software in the Adaptive Precorrector board.

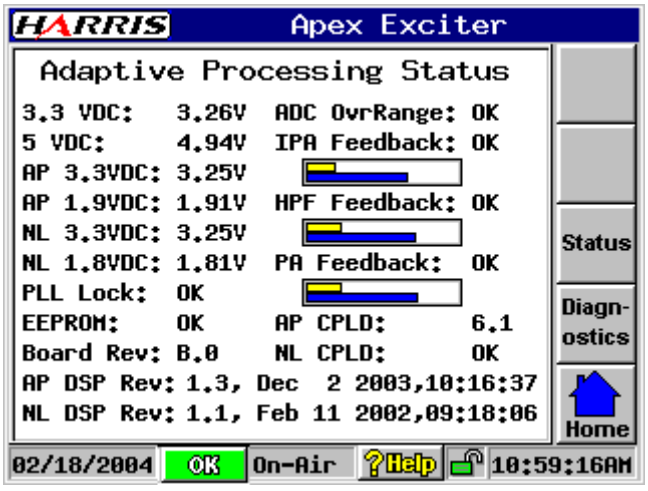

Figure 3-8 Adaptive Processing Board Status Screen

WARNING: Disconnect primary power prior to servicing.

3.4.3.1 Adaptive Processing Diagnostics

The Adaptive Processing Diagnostic screen is shown in Figure 3-9, with screen entries listed below.

- loopback: Selections include None, Analog, or Digital.

  None is the normal mode.

  Digital loops the D/A converter input bit stream back to replace the A/D converter output bit stream. It tests the modulator and corrector boards.

  Analog loops the 10.762 MHz IF output from the D/A board to the IF input of the A/D board via an existing RF cable jumper. It tests the A/D and D/A converters.

  > Results of the digital or analog loopbacks can be viewed on the Main screen response display by setting the Setup > Display Setup Chart Source selection to exciter, and on the eye pattern by setting Main screen - RTAC - Lin HPF to Adapt.

- Test Tones: (Disabled or Enabled) Disabled is normal mode. Enabled turns on two test tones, which are used as built in functions for inter modulation tests. It is used by factory final test and field service. When enabled, this function mutes the exciter, the signals are visible within the exciter.

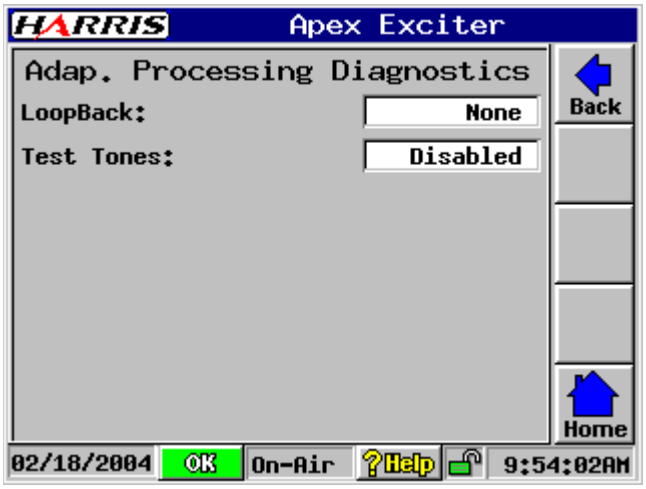

Figure 3-9 Adaptive Processing Diagnostics

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3.4.4 Digital Processing Screens

The Digital processing Status selection contains two sub screens, which are:

- Modulator Board, Screen 1 of 2
- ADC & DAC Boards, Screen 2 of 2.

3.4.4.1 Modulator Board Status Screen

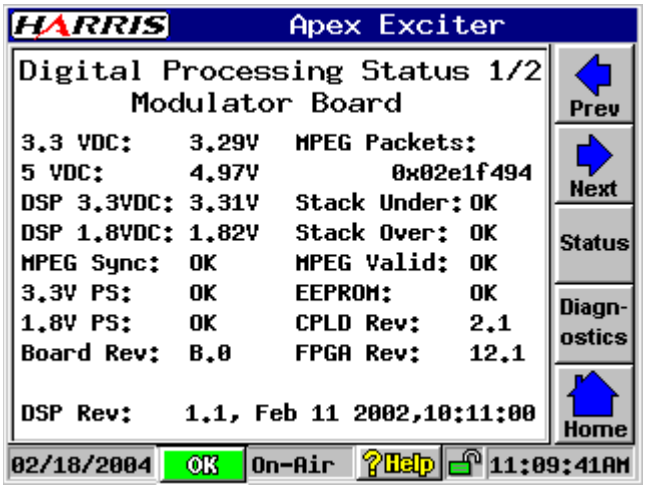

Figure 3-10 Modulation Board Status Screen

The Modulation Status screen is shown in Figure 3-10, with screen entries listed below.

- 3.3 Vdc: This is the output of the 3.3 V dc to dc converter.

  3.3 Vdc from this board is supplied to the SMPTE 310 Interface board.
- 5 Vdc: This is the board input voltage, which comes from the controller board.
- DSP 3.3 Vdc supply is derived from the 3.3 Vdc supply through an FET switch. This voltage is switched off if the DSP 1.8 Vdc supply faults.
- DSP 1.8 Vdc This is the output of the 1.8 volt core power supply.
- MPEG Sync: (OK or FAULT) indicates MPEG sync is locked to the transport stream signal input of the SMPTE board.

  Fault is indicated if no MPEG input is provided and exciter setup screen > SMPTE Test Pattern is set to off.
- 3.3 V PS: (OK or FAULT) refers to the output of the 3.3 volt dc to dc converter.
- 1.8 V PS: (OK or FAULT) refers to the output of the DSP 1.8 volt supply.
- Board Rev: Board revision level for the Modulator board.
- CPLD Rev: Revision level of the CPLD in the Modulator board.
- FPGA Rev: Revision level of the firmware in the field programmable gate array in the Modulator board.
- MPEG Packets: This continuously changing display is a count of the MPEG packets.
- Stack Under: (Ok or FAULT)
- Stack Over: (Ok or FAULT)

The Stack is a memory that buffers the input to the Modulator board DSP. Various interrupts cause the DSP to momentarily stop processing the transport stream data while it performs other tasks. The incoming transport stream data is stored in the stack memory while it is waiting for the DSP to process it. The DSP processing speed is such that the stack should never get full (over range) or empty (under range). This ensures a steady flow of transmission data from the modulator board.

- MPEG Valid: (Ok or FAULT) This entry tells if the MPEG signal from the SMPTE board is good. It can be compared to the SMPTE Output Lock entry of the MPEG Input Status board to help isolate problems.

  Fault is indicated if no MPEG input is provided and exciter setup screen > SMPTE Test Pattern is set to off.
- EEPROM: (Ok or FAULT) The EEPROM is the local board memory. It stores board specific information such as board revision, CPLD revision, FPGA revision, and other local data.
- DSP Rev: This is the revision level of the modulator board digital signal processor.

3.4.4.1.1 Modulator Diagnostics

The Modulator Diagnostics screen is shown in Figure 3-11, with screen entries listed below.

- Nyquist Filter Data: (Disabled or Enabled) Enabled is the normal mode of operation. Disabled causes the exciter to output a CW tone at the pilot frequency.

Caution

Operating at full power with only the pilot may damage the transmitter power amplifier. Reduce transmitter output power or disconnect exciter RF output from transmitter before performing this test.

- Nyquist Test Pattern (3 tone): (Disabled or Enabled) Disabled is normal. When Enabled, a test pattern consisting of three tones is generated in the FPGA on the modulator board. This confirms correct operation from the output of the modulator board. It can also be used for inter modulation tests.

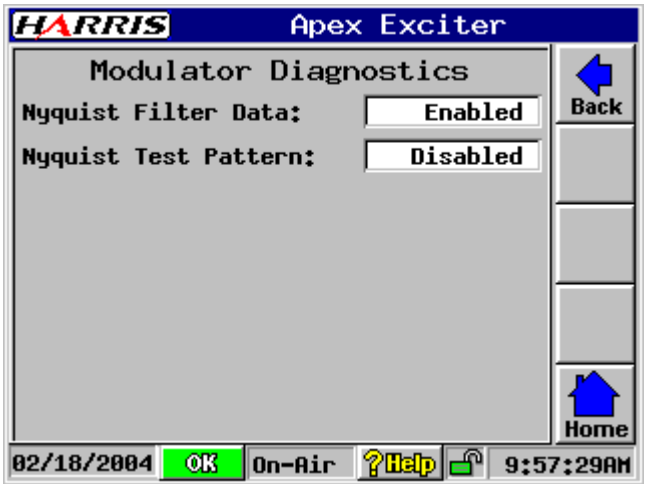

Figure 3-11 Modulator Diagnostics

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3.4.4.2 ADC and DAC Boards Status Screen

Refer to Figure 3-12. The ADC and DAC screen entries are listed below.

- ADC Board Rev: This is the board revision for the analog to digital converter board.
- DAC Board Rev: This is the board revision for the digital to analog converter board.

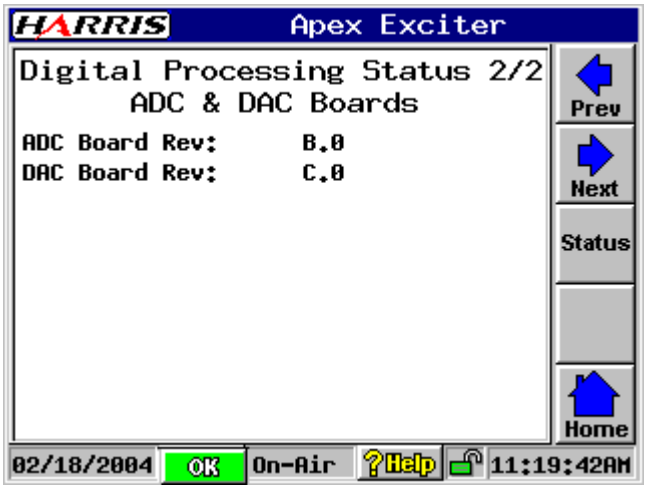

Figure 3-12 ADC and DAC Status Screen

3.4.5 IF & RF Processing Status Screens

The IF & RF Processing Status selection contains four sub screens, which are:

- UDC Interface Board, Screen 1 of 4
- PLL Board, Screen 2 of 4.
- Up Converter Board, Screen 3 of 4.
- Down Converter Board, Screen 4 of 4.

3.4.5.1 UDC Interface Board Status Screen

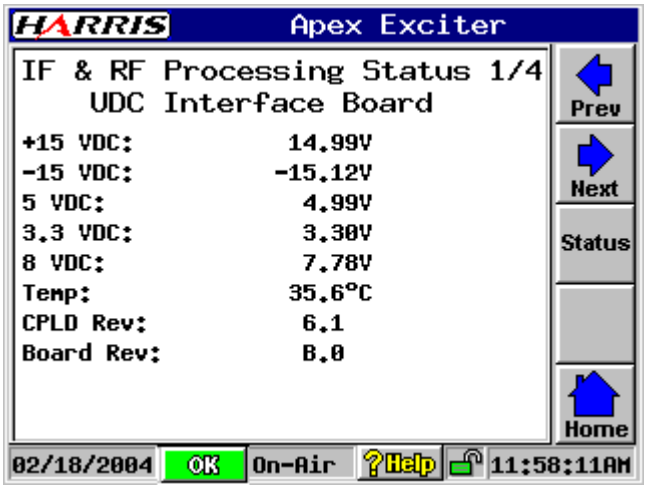

Figure 3-13 UDC Interface Board Status Screen

WARNING: Disconnect primary power prior to servicing.

The UDC Interface Board screen is shown in Figure 3-13, with screen entries listed below.

- 15 Vdc: Input from power supply module
- -15 Vdc: Input from power supply module
- 5 Vdc: Output from 5 volt linear regulator chip U4.
- 3.3 Vdc: Output from 3.3 volt linear regulator chip U6.
- 8 Vdc: Output from 8 volt switching regulator
- Temp: This is the ambient air temperature inside the analog (top) side of the exciter.
- CPLD Rev: This is the revision level of the CPLD in the UDC Interface board.
- Board Rev: This is the board revision for the UDC Interface board.

3.4.5.2 PLL Board Status Screen

The PLL Board screen is shown in Figure 3-14, with screen entries listed below.

- 15 Vdc: Input power from UDC interface board via connector J1.
- -15 Vdc: Input power from UDC interface board via connector J1.
- 8 Vdc: Input power from UDC interface board via connector J1.
- IF PLL Lock: (YES or NO) This PLL should normally be locked.
- RF PLL Lock: (YES or NO) This PLL should normally be locked.
- 10MHz PLL Lock: (YES or NO) This PLL is locked if external reference is present. Lock occurs approximately one minute after external 10 MHz is connected.
- Ext. Reference: (YES or NO) Reads YES if external reference is present.
- Board Rev: This is the board revision for the PLL board.

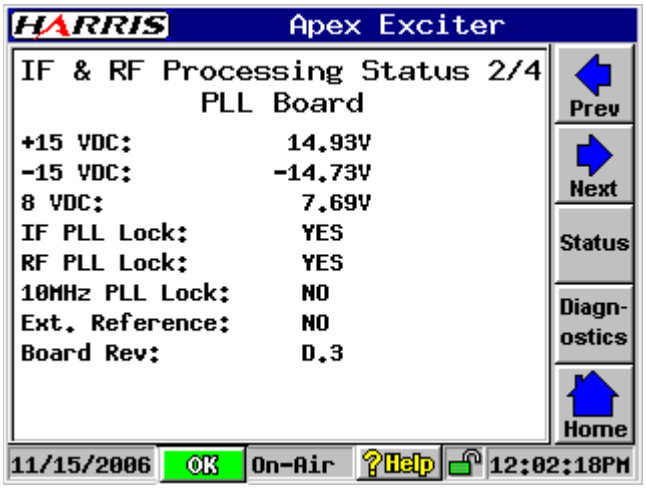

Figure 3-14 PLL Board Status Screen

WARNING: Disconnect primary power prior to servicing.

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3.4.5.2.1 PLL Diagnostics

Refer to Figure 3-15. This screen has an Xtal Aging (crystal oscillator aging) control. It is used to set the frequency of the internal 10 MHz crystal oscillator. The initial setting should typically be in the range of 3000 to 3500. The 10 MHz crystal adjustment process is given in Section 5.1.3, Measuring and Setting Pilot and PLL Board Frequencies on page 5-7.

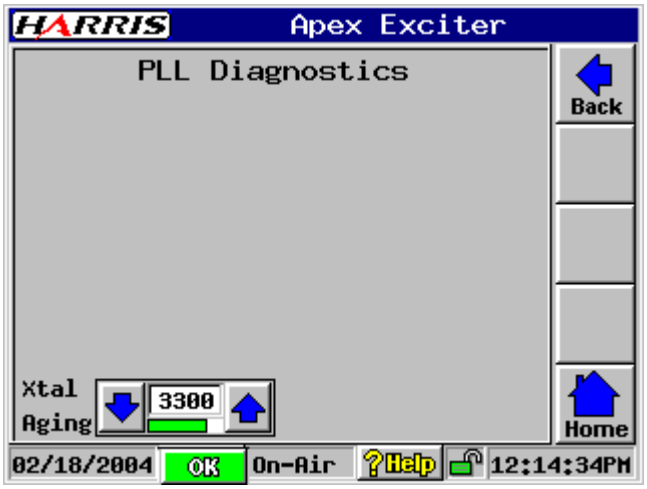

Figure 3-15 PLL Diagnostics

3.4.5.3 Up Converter Board Status Screen

The exciter output amplifier does not have a separate screen. It parameters (+/-15 Vdc and RF detector output) are included in this screen. The UDC Interface Board screen is shown in Figure 3-16, with screen entries listed below.

- 15 Vdc: Input power from UDC interface board via connector J3.
- -15 Vdc: Input power from UDC interface board via connector J3.
- 8 Vdc: Input power from UDC interface board via connector J3.
- RF Detector: Rectified RF output voltage sample from exciter output amplifier.
- Board Rev: This is the board revision for the Up Converter board.

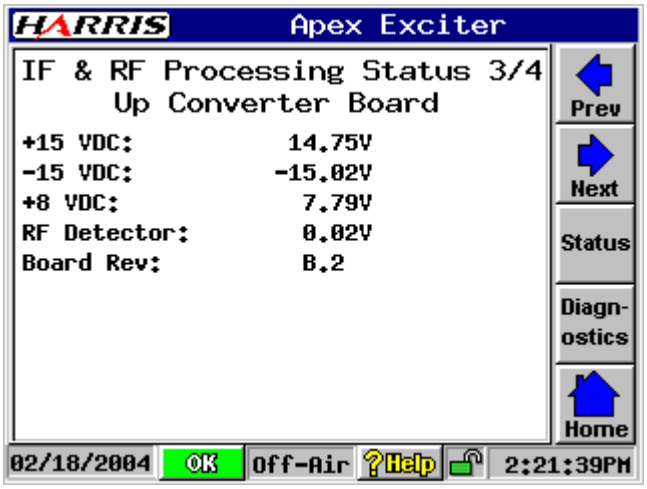

Figure 3-16 Up Converter Board Status Screen

WARNING: Disconnect primary power prior to servicing.

3.4.5.3.1 Up Converter Diagnostics

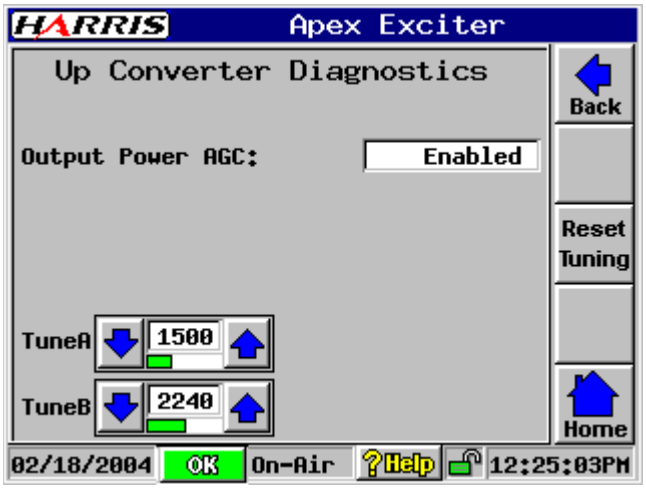

Figure 3-17 Up Converter Diagnostics

The Up Converter Diagnostics screen is shown in Figure 3-17, with screen entries listed below.

- Output Power AGC. When enabled, the exciter output power level is set from the exciter main screen or the extended control. This is the normal setting.

  When disabled, for test purposes, the exciter output power is locked in the previous (enabled) AGC setting. This is a good mode for testing the analog tray RF circuits, because the RF level will remain constant when an RF cable is disconnected.

- TuneA: (range 0 to 4095) The number in the TuneA window represents the dc voltage applied to the UHF tunable notch filter in the up converter. This voltage places the notch at the local oscillator frequency to improve local oscillator rejection in the exciter RF output signal. The initial values for all channels are stored in the exciter. Adjustment is not required. In the UHF band, the local oscillator is 140 MHz below the center of the channel and in the VHF band, the local oscillator is 140 MHz above the center of the channel.

  Using the up or down arrows, this voltage can be changed to change the notch filter tuning. Increasing the number increases the notch frequency. This test is performed, while observing the exciter RF output on a spectrum analyzer.

- TuneB: (range 0 to 4095) The number in the TuneB window represents the dc voltage applied to the UHF tunable bandpass filter in the up converter. This voltage places the selected transmitting channel in the center of the bandpass of the filter. The initial values for all channels are stored in the exciter. Adjustment is not usually required.

  Using the up or down arrows, this voltage can be changed to change the filter tuning. Increasing the number increases the filter center frequency. Filter tuning is checked with RTAC correction bypassed, while observing the exciter RF output on a spectrum analyzer. If the filter is tuned slightly off center channel, the 8-VSB response will tilt and the EVM (error vector magnitude) will increase.

- Reset Tuning: When pressed, this soft key will restore the default values to tune A and tune B. When tune A and/or tune B values are changed, they are automatically saved and will not revert to the default values after the exciter is momentarily powered down.

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3.4.5.4 Down Converter Board Status Screen

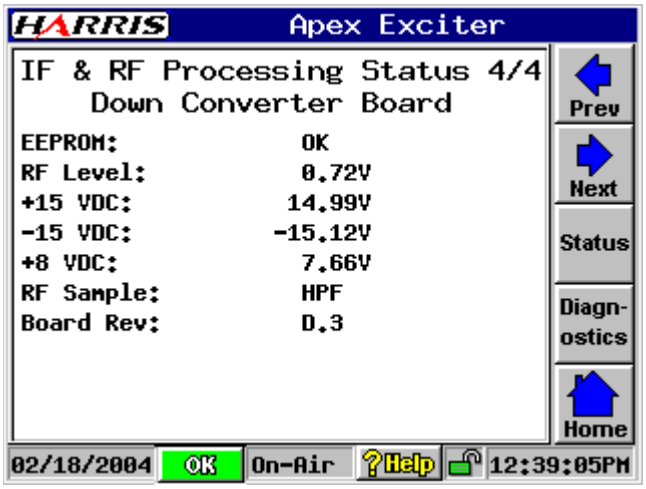

Figure 3-18 Down Converter Board Status Screen

For the IPA, PA, and HPF samples, the RF level for each sample should be within a range of -10 to 0 dBm average power.

The following ia a list of entries on the External I/O Status Screen, refer to Figure 3-18.

- EEPROM: (Ok or FAULT) The EEPROM is the local board memory. It stores board specific information such as board revision, CPLD revision, and other local data.
- RF Level: This is the RF level (taken after the AGC circuit) of the current sample. It typically ranges between 0.6 to 1.0 Vdc when samples of proper power range are present at the inputs.
- +15 Vdc: Input power from UDC interface board via connector J8.
- -15 Vdc: Input power from UDC interface board via connector J8.
- 8 Vdc: Input power from UDC interface board via connector J8.
- RF Sample: This displays the name of the RF sample source (Exciter, IPA, Amplifier, and HPF).

  These samples normally cycle through in two to four second steps. The sequence is IPA, HPF, Amplifier, and HPF.
- Board Rev: This is the board revision for the Down Converter board.

3.4.5.4.1 Down Converter Diagnostics

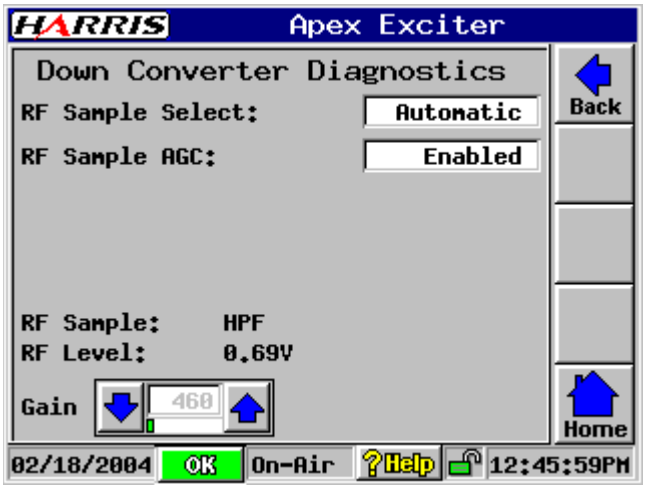

Figure 3-19 Down Converter Diagnostics

The down converter has four inputs, which are RF output samples of the exciter, transmitter IPA, transmitter PA, and HPF (high power filter). The exciter input is an internal loopback from the output amplifier. The controller board causes the down converter to switch through these samples. The IPA and PA samples take up to 5 seconds each and the HPF takes 5 to 90 seconds depending on the length and type of waveguide entered in the exciter setup page. The exciter is only sampled when the Setup > Display > Chart Source is set to monitor the exciter. During each sample period, the first action is to adjust the down converter gain to provide the A/D converter with an IF signal of the correct amplitude. During the remainder of the sample, RTAC acts on the sample to produce the appropriate precorrection.

The Down Converter Diagnostics screen is shown in Figure 3-19, with screen entries listed below.

- RF Sample Select: (Automatic, Exciter, IPA, Amplifier, or HPF.

  The RF sample select must be set to automatic for RTAC to properly correct the transmitter system output.

  When Automatic is selected, the controller board causes the down converter to switch between the IPA, Amplifier, and HPF inputs in the following order. IPA, HPF, Amplifier, then HPF again. The exciter is only sampled when the Setup > Display > Chart Source is set to monitor the exciter.

  When not in automatic mode, the input to the down converter is locked to Exciter, IPA, Amplifier, or HPF. When one of the input samples is selected, that sample is internally routed to the IPA, HPF, and PA feedback inputs, shown in the adaptive processing status screen, and is therefore used by RTAC to set the linear and non-linear correction. This mode is useful for troubleshooting diagnostics.

- RF Sample AGC: (Enabled or Disabled), actually an APC, automatic power control.

  When enabled, the level of each RF sample (at the output of the down converter) is adjusted to the correct level required at the input of the ADC (analog to digital converter). It should remain enabled to keep the IF sample signals to the A/D converter at a constant level.

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When disabled, for test purposes, the level of each RF sample (at the output of the down converter) is set by the blue up and down gain arrows at the bottom of the screen. The possible range is 0 - 4096. Sample levels can be viewed on the Adaptive Processing Screen.

- RF Sample tells which down converter RF input sample is currently active.
- RF Level: This is the RF level (taken after the AGC circuit) for the current sample. It typically ranges between 0.6 to 1.0 Vdc when samples of proper power range are present at the inputs.
- Gain: This control is only active when RF Sample AGC (on this screen) is defeated. It is used to set the down converter gain so that the sample level falls between 0.6 and 1.0 Vdc. When RF Sample AGC is enabled the gain required for the active sample is shown in the “washed out” mode.

3.4.6 System Control Status Screens

The IF & RF Processing Status selection contains four sub screens, which are:

- Controller Board, Screen 1 of 4
- External I/O Board, Screen 2 of 4.
- CAN Status, Screen 3 of 4.
- Front Panel Board, Screen 4 of 4.

3.4.6.1 Controller Board Status Screen

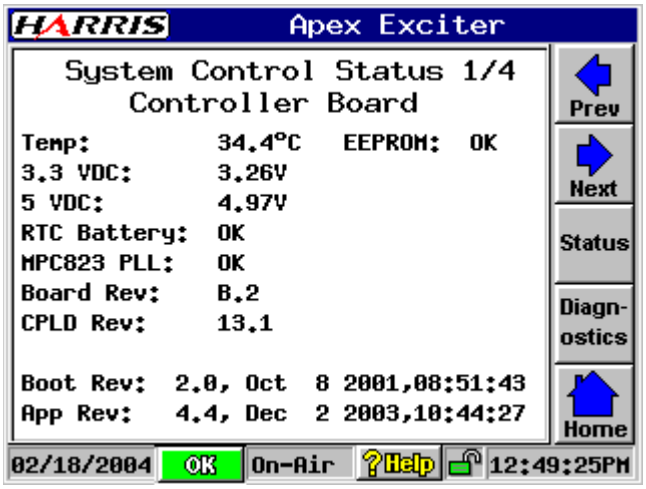

Figure 3-20 Controller Board Status Screen

The Controller Board screen is shown in Figure 3-20, with screen entries listed below.

- Temp: This is the ambient air temperature of the digital (bottom) side of the exciter.
- 3.3 Vdc: This is the output of the 3.3 V dc to dc converter.
- 5 Vdc: This is the board input voltage from the main power supply.
- RTC battery: (OK or FAULT) Fault means battery is low and needs replaced.

WARNING: Disconnect primary power prior to servicing.

- MPC823 PLL: (Ok or FAULT) This is the lock status of the internal PLL of the MPC823 micro controller on the controller board. It indicates the internal 75 MHz clock is locked to the 32.768 KHz crystal oscillator.
- EEPROM: (Ok or FAULT) This EEPROM is used to save the user entered menu selection from the various LCD screens.
- Board Rev: Board revision for the Controller board.
- CPLD Rev: Revision level of the CPLD in the controller board.
- Boot Rev: Boot code revision level for the controller board.
- APP Rev: Micro controller application code revision level on the controller board.

3.4.6.1.1 Controller Board Diagnostics

A Bit Fifo Test Pattern function is available on the Controller Board Diagnostics screen. This function is used by engineering and must remain disabled. If enabled, it will block the normal 8-VSB signal flow.

3.4.6.2 External I/O Board Status Screen

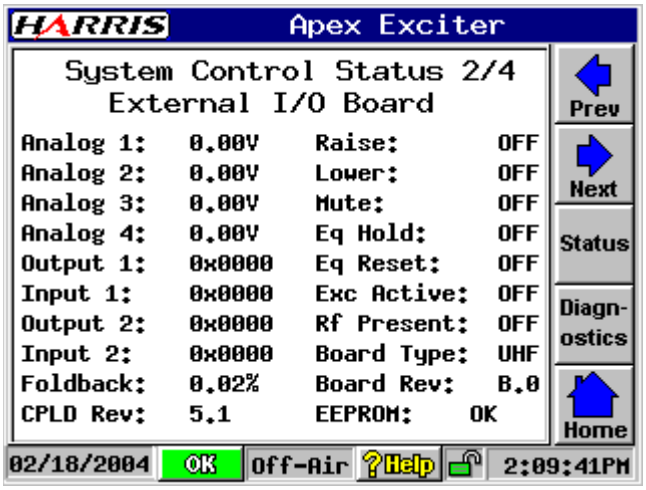

Figure 3-21 External I/O Board Status Screen

The External I/O Board Status screen is shown in Figure 3-21, with screen entries listed below. These entries represent the command inputs and the status and analog outputs that enter and leave connector J1 of the external I/O board at the rear of the exciter.

- Analog 1: 0.000V refers to analog input 1.
- Analog 2: 0.000V refers to analog input 2.
- Analog 3: 0.000V refers to analog input 3.
- Analog 4: 0.000V refers to analog input 4.
- Output 1, Input 1, Output 2, and Input 2.

  These are binary representations of the 16 digital input/output status channels. They refer to the fact that 2 - 16 bit registers are required to handle the 16 status channels. These entries are used for factory testing.

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- Foldback: This in an analog input which tells the percent of exciter output power foldback, typically due to transmitter PA VSWR exceeding a preset level.

  When VSWR foldback is active the foldback readout on the External I/O status page will be yellow.
- Raise: (OFF or ON) When on, this input commands the exciter output power to raise.
- Lower: (OFF or ON) When on, this input commands the exciter output power to lower.
- Mute: (OFF or ON) Exciter RF output amplifier mute function status.
  Off mode allows RF to flow through the output connector (J2) to the transmitter.
  On (enabled) switches the RF output to connector J3, which has a test load.
  In either mode a sample of the output is available at connector J4.
- EQ Hold: (Off or On) When on, this input places the three adaptive equalizer inputs, shown on the main screen, to hold. This holds the adaptive equalizer (RTAC) to the settings that existed when the hold command was given.
- Eq Reset: (Off or On) Normally off, when momentarily turned on the adaptive equalizer will be reset.
- Exc Active: (Off or On) When on, this exciter is on the air.
- RF Present: (Off or On) This is an indication that the RF level at the output of the exciter is above a given threshold level. The RF presence threshold is an RF output level of approximately 5 mW.
- Board Type: (UHF or VHF) Interface configured to fit existing UHF and VHF exciter interface connections.
- Board Rev: This is the board revision for the External I/O board.
- CPLD Rev: This is the software revision level of the CPLD in the External I/O board.
- EEPROM: (Ok or FAULT) The EEPROM is the local board memory. It stores board specific information such as board type, board revision, CPLD revision, and other local data.

Note

Within any of these screens, touching Home returns to the main screen, and touching Fault brings up the Exciter Status screen.

3.4.6.2.1 External I/O Diagnostics

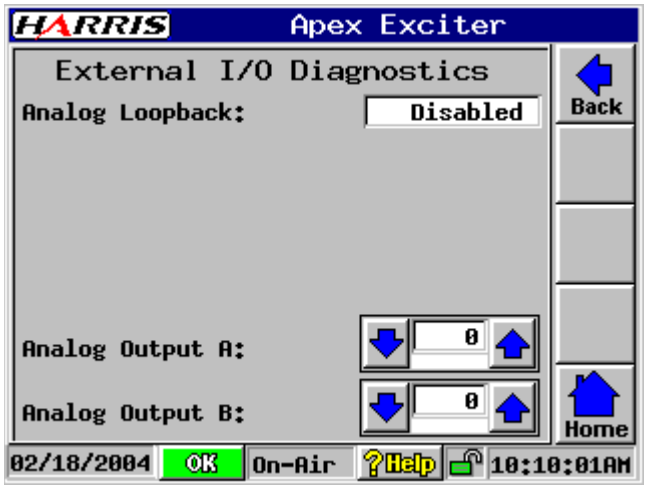

Figure 3-22 External I/O Diagnostics

The External I/O Diagnostics screen is shown in Figure 3-22.

Analog loopback: Choices are Enabled or Disabled. Disabled is the normal setting.

- This function loops an analog output back through an analog input channel for diagnostics purposes.

The last two screen entries are Analog Output A and Analog Output B. These two entries provide a voltage for the analog loopback test mentioned above.

- Analog Output A is looped back through analog Analog 1 and 3 inputs and Analog Output B is looped back through Analog 2 and 4 inputs, see external I/O Board screen Figure 3-21 for the analog inputs.
- For both of these entries the selectable range, entered on the touch screen number pad, is 0 to 4095. The number selection represents a dc voltage in millivolts. For example, a setting of 3000 represents 3000 mVdc or 3 Vdc.
- These analog channels have a total of four inputs and two outputs for the UHF External I/O board and two inputs and two outputs for the VHF External I/O board.

When performing the loopback test, the results appear on the External I/O board status screen, Figure 3-21. The analog output A and B voltages appears on the appropriate analog 1 through 4 inputs. Analog 1 input also appears by the foldback entry as a percentage.

For example, if analog loopback is enabled and analog output A is set for 2000 and B is set for 3000, analog inputs 1 and 3 will measure within a few tenths of a volt of 2 Vdc, analog inputs 2 and 4 will measure within a few tenths of a volt of 3 Vdc. The VSWR foldback percentage will be based on the relative value of the loopback voltage (V_{LB}) compared to the External I/O setup screen low voltage (V_{LT}) and high voltage (V_{HT}) VSWR foldback thresholds.

$$\text{Foldback Percentage} = \frac{V_{LB} - V_{LT}}{V_{HT} - V_{LT}} \times 100$$

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The analog loopback function produces outputs at various pins of J1, the pinout is as follows:

- When analog output A is set to a value, such as 2500, 2.5 Vdc will appear at the analog 1 output, which is J1 pin 4 for UHF and J1 pin 7 for VHF. This output is present if loopback is enabled or disabled and the connection to J1 has a high impedance.
- When analog output B is set to a value, such as 3000, 3.0 Vdc will appear at the analog 2 output, which is J1 pin 17 for UHF and J1 pin 8 for VHF. This output is present if loopback is enabled or disabled and the connection to J1 has a high impedance.
- When loopback is enabled, the voltage set by analog output A or B is present at the appropriate analog input J1 connectors.

  The pinouts for UHF analog inputs 1 through 4 are J1-12, J1-13, J1-3, and J1-16 respectively.

  The pinouts for VHF analog inputs 1 and 2 are J1-15 and J1-16 respectively.

3.4.6.3 CAN Bus Status Screen

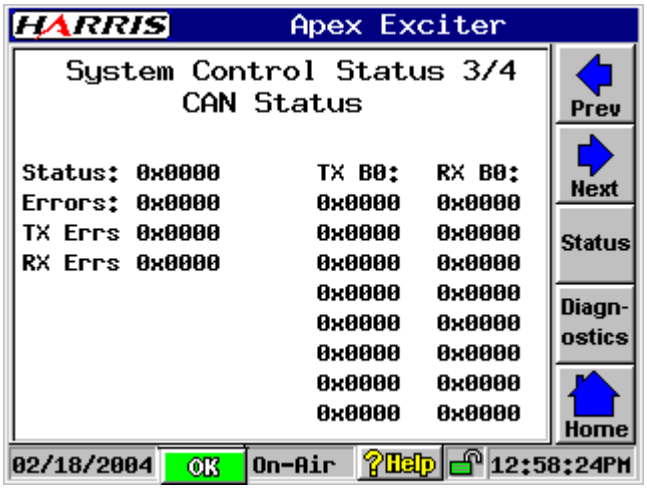

Figure 3-23 CAN Bus Status Screen

3.4.6.3.1 CAN Diagnostics

A CAN Test Message is available on the CAN Diagnostics screen. This function is used by engineering and must remain disabled.

3.4.6.4 Front Panel Board Status Screen

This screen gives the board revision and CPLD revision for the front panel board.

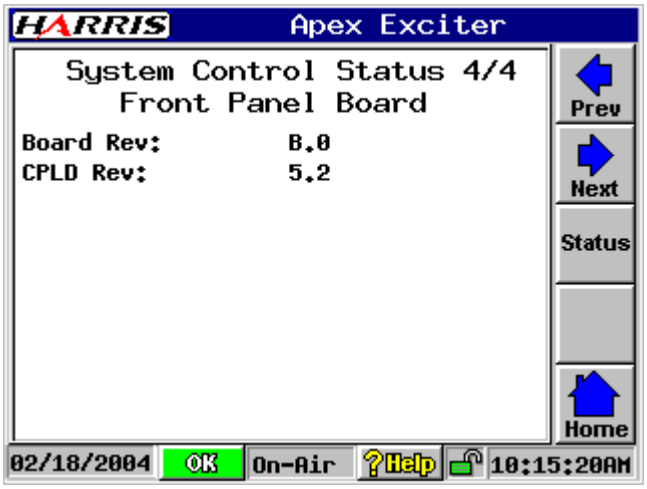

Figure 3-24 Front Panel Board Status Screen

3.5 Built In Tests

The BIT (built in tests) soft key is found on the right side of the System Status screen, shown in Figure 3-5. When the BIT soft key is pressed, see Figure 3-25, a sub window appears. The message in this window is “Starting BIT requires exciter to be muted.” If the Ok soft key is pressed, the exciter RF output is reduced to zero. If the cancel soft key is pressed the exciter continues to function in the previous mode. When the Built In Test screen is exited, the exciter operation resumes in its previous mode.

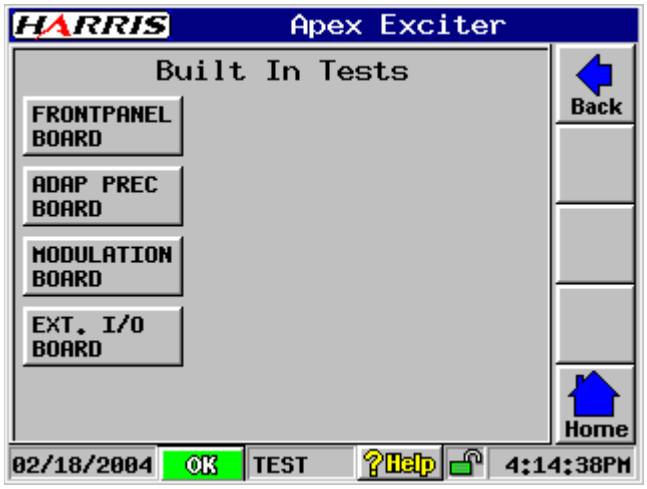

Figure 3-25 Built In Tests Screen

WARNING: Disconnect primary power prior to servicing.

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3.6 Details of the System Setup Screens

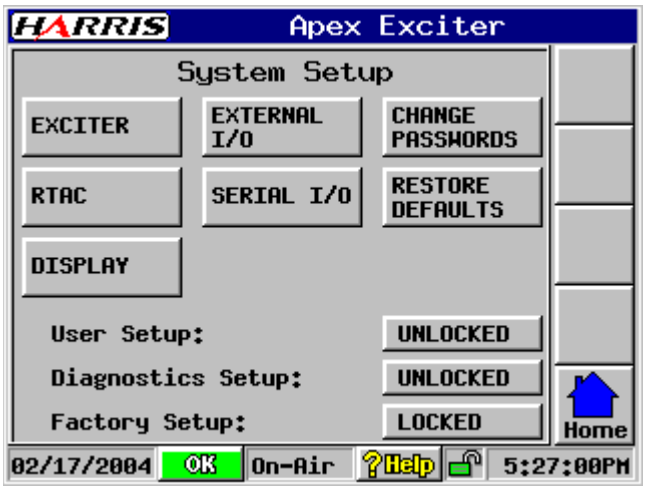

Figure 3-26 System Setup Screen

This section provides pictures and details of the series of exciter setup screens. Section 3.3 on page 3-4 provides general information about interconnecting structure of the screens.

If the User Setup is locked, all setup functions and the exciter power raise and lower functions will be locked and their various setup screen selection values will be greyed out. Only the Exciter Setup screen Channel and Frequency Offset functions and the change Diagnostics password will be available.

Refer to Figure 3-26. Touching any of the eight boxes on the System Setup screen brings up the setup sub screen for that area, see Table 3-2 to find the page numbers for the sub screens. Within any of these screens, touching Home returns to the main screen, touching back returns to the System Setup screen, and touching Fault (at the bottom of the screen, visible only if a fault exists) brings up the System Status screen. See Figure 3-4, on page 3-7 for a view of the exciter LCD display flow chart.

When a numeric entry is needed, touching that entry causes a numerical touch pad is displayed. This pad has numbers from 0 to 9, a decimal point, and a +/- selection.

An alpha numeric key pad is displayed when a title is needed.

Table 3-2 Location of System Setup Sub Screens

Choice	**Location**
Exciter	Exciter Setup Screens, on page 3-28
RTAC Filters	RTAC Setup Screen, on page 3-32
Display	Display Setup Screen, on page 3-34
External I/O	External I/O Setup Screen, on page 3-35
Serial I/O	Serial I/O Setup Screens, on page 3-40
Change Passwords	Change Passwords > Security Setup, on page 3-43
User Setup:	User Setup (Locked or Unlocked), on page 3-44
Diagnostics Setup:	Diagnostics Setup (Locked or Unlocked), on page 3-44
Factory Setup:	Factory Setup (Locked or Unlocked), on page 3-45
Restore Defaults	Restore Defaults, on page 3-45

WARNING: Disconnect primary power prior to servicing.

3.6.1 Exciter Setup Screens

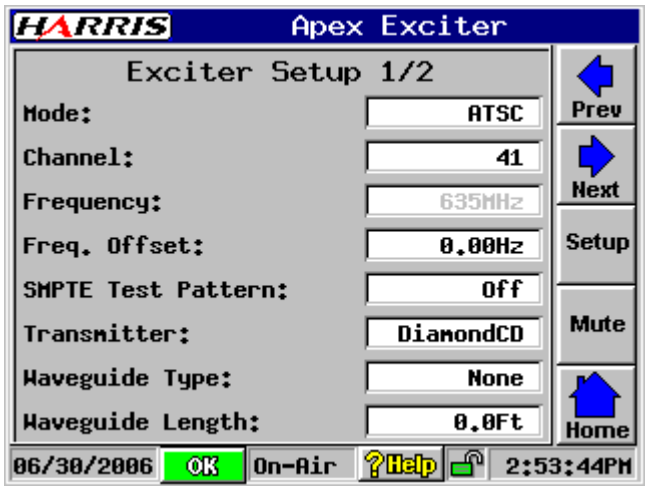

Figure 3-27 Exciter Setup Screen 1 of 2

Refer to Figure 3-27, Exciter Setup Screen 1 of 2. The following ia a list of entries on the Exciter setup screen 1 of 2.

- Mode: ATSC is the only active mode at this time, therefore, the mode window is displayed in the washed out mode.
- Channel: Enter the channel number (from channel 2 through channel 69)

  The channel box will be greyed out (and unattainable) if the diagnostic setup feature is locked. Instructions to lock or unlock the diagnostics setup is found in Section 3.6.6.2, Diagnostics Setup (Locked or Unlocked) on page 3-44.

  A warning prompt is displayed when the channel change option is entered. This is intended to discourage accidental damage to transmission systems.
- Frequency: The center frequency for the channel number (selected above) will automatically be displayed. Presently, the display is shown in the “washed out” mode.
- Freq. Offset: Enter the desired pilot frequency offset (in hertz). The maximum limits which can be entered as a frequency offset is +/-50 kHz.

  The pilot frequency offset box will be greyed out (and unattainable) if the diagnostic setup feature is locked. Instructions to lock or unlock the diagnostics setup is found in Section 3.6.6.2, Diagnostics Setup (Locked or Unlocked) on page 3-44.
- SMPTE Test Pattern: Choices include Off, All 0’s, All 1’s, Hex 80, Ramp, PN23, and Loopback.

  A valid SMPTE 310 transport stream can be generated internally by selecting one of the test patterns (except Loopback) in the SMPTE Test Pattern selection of the Exciter Setup screen.

If a test pattern is selected, with or without a valid SMPTE 310M signal present at the exciter input, the SMPTE Input Lock will still show fault but the SMPTE Output Lock and the Modulator board (located under Digital Processing Status) should show no faults.

- All 0's: All the bits of each byte of a packet, except the sync byte, is 0
- All 1's: All the bits of each byte of a packet, except the sync byte, is 1
- Hex 80: Every byte except the sync byte is the hexadecimal number 80
- RAMP: This signal is a sequence of bytes counting from 1 to 187.
- PN23: This is a continually generated -random number sequence of 2^{23} - 1 bits. This stream replaces the 187 bytes of a packet with the PN23 sequence.

  A PN23 test set analyzes the demodulated transmission stream which contains the PN23 test signal and flags any bytes which contain errors.
- loopback: This is a loop between the modulator and the SMPTE boards. The modulator sends data to the SMPTE board, which sends it back to the modulator where it is compared with the date that was sent.

  Loopback is used primarily during the Modulator board BIT (built in tests).

- Transmitter: Select the transmitter type from the display that appears. Choices are:

  DiamondCD (Harris Diamond series UHF digital transmitter)

  PowerCD (Harris series MEDC IOT series UHF digital transmitter)

  SigmaCD (Harris Sigma series UHF digital transmitter)

  PlatinumCD (Harris Platinum series VHF digital transmitter)

  Custom (for other digital TV transmitters)

  Ranger (Harris Ranger series UHF digital transmitter)

- Waveguide Type: For UHF channels, enter the type of waveguide used between the HPF and the antenna.

  Selecting a type (and length) of waveguide allows RTAC to pre correct for waveguide group delay. Selecting None provides no waveguide group delay precorrection.

  If the wrong type of waveguide is selected for the operating channel, no group delay precorrection will be applied.

  Available choices are:

  None

  WR1800, rectangular, for channels 14 through 35

  WR1500, rectangular, for channels 20 through 56

  WR1150, rectangular, for channels 46 through 69

  GLW1750, circular, for channels 14 through 19 and 24 through 41

  GLW1700, circular, for channels 20 through 23

  GLW1500, circular, for channels 39 through 55.

  GLW1350, circular, for channels 56 through 69.

- Waveguide Length: Enter the length of waveguide (up to 2000 feet) used between the HPF and the antenna. Length is needed, in addition to selecting waveguide type, to allow RTAC to pre correct for waveguide group delay.

WARNING: Disconnect primary power prior to servicing.

Mute (soft key on right side of screen)

- Mute: (Enabled or Disabled) When Enabled, the exciter RF output is switched to an internal load. When Disabled, RF is present at the exciter RF output connector.

  In either mode the exciter is capable of performing self tests which involve the RF output of the exciter. This provides a test of the up converter, down converter, and output amplifier. This loopback can be viewed by selecting Exciter from the Chart Source selections of the Setup > Display > Display Setup screen.

  The RF Mute status of the exciter is displayed on the at the bottom of all screens. It will indicate On-Air, Off-Air, or Mute.

  If the exciter stays muted when attempting to unmute from the exciter setup screen, check the mute status on the System Control Status 2/4, External I/O Board. If it indicates On, a mute command is being sent to the external I/O board via connector J1

3.6.1.1 Exciter Setup Screen 2 of 2, Power Limit and Calibration

Refer to Figure 3-28, Exciter Setup Screen 2 of 2. The following ia a list of entries on the Exciter setup screen 2 of 2.

- Power Limit. This adjustable S/W power limit will act as a clamp and will not allow the user to set the power above this limit either locally on the exciter main screen or remotely via the external I/O board raise/lower input.
- Power Cal (calibration) soft key on the right side of the screen activates the exciter RF output power calibration procedure. This procedure is covered in section Section 3.6.1.2, Power Calibration, on page 3-31.

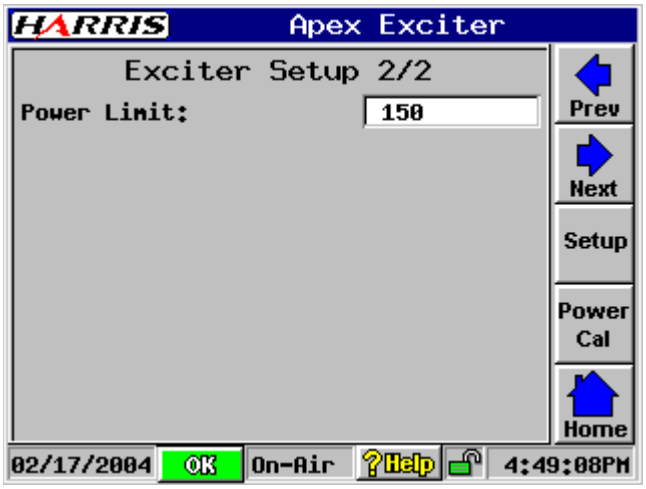

Figure 3-28 Exciter Setup Screen 2 of 2

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3.6.1.2 Power Calibration

Power Cal (calibration) soft key on the right side of the screen in Figure 3-28 activates the exciter RF output power calibration procedure. The power calibration is accomplished by connecting an accurate power meter to the RF output of the exciter and pressing the blue up or down arrows (see Figure 3-29) until the power meter reads 250 mW average power. Then press the Accept button to implement the new calibration or press the cancel button to return to the old calibration.

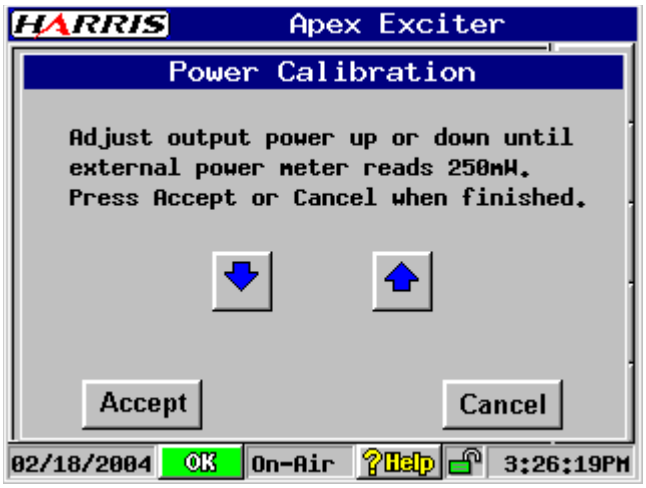

Figure 3-29 Power Calibration Screen

3.6.2 RTAC Setup Screen

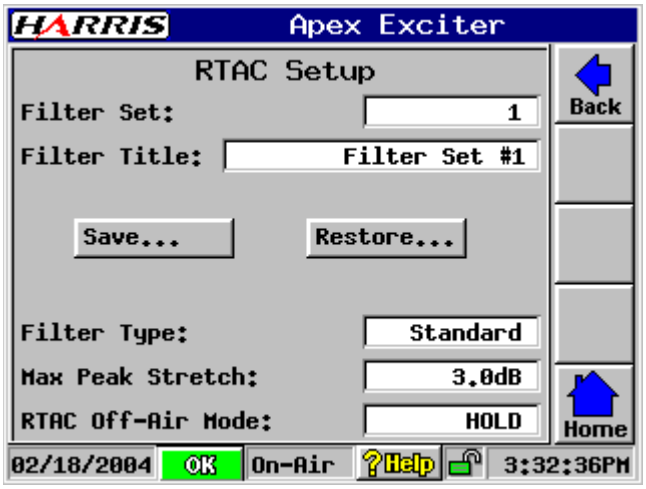

Figure 3-30 RTAC Setup Screen

Up to four Existing RTAC correction setups can be saved as RTAC filter sets. An option to name each saved filter setup exists. Filter setups can be stored for many reasons, such as when the transmitter was first installed, after transmitter maintenance, and etc. They are good for comparative testing.

- Filter Set: (selections include 1 through 4)
- Filter Title: Brings up an alpha/numeric touch keypad to enter the name for the selected filter set.
- Save: Pressing this soft key saves the current RTAC correction algorithm to the filter set selected.

  The filter set should be given a name (in the filter title selection).
- Restore: Pressing this soft key applies the selected, pre-saved correction algorithm filter set to the RTAC correction algorithm.

  This causes the Main screen RTAC samples to be set to Default, which applies the pre-saved filter set to the RTAC correction algorithm.

3.6.2.1 Filter Type

Channel 14 digital transmitters may interfere with land mobile radio systems operating immediately below channel 14 and therefore require a special HPF (high power filter). Precorrection is required to enable RTAC to correct the linear distortions of these filters.

The Setup > RTAC Setup > Filter Type: CH 14 Super applies the necessary amplitude response and group delay precorrection, which reduces the distortions within the correction range of the RTAC circuits. Selecting the correct filter improves the correction and speeds the initial automatic setup time. Choices are:

- **Standard:** This selection is used if the transmitter system includes the standard D-Mask filter.
- **Asymm STF:** Use this if the transmitter system uses the sharp tuned filter (sometimes called “Cool Fuel”) it also is used when the group delay for the transmitter is not symmetrical, such as when its output is reflected through an adjacent channel sharp tuned filter in order to combine the two transmitters.

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- **CH 14 Super:** Use this selection only if the system includes a special high power filter used to protect land mobile operators on frequencies immediately below ch 14.
- **The Exciter must be restarted** to make filter change active.

Caution

If the CH 14 Super selection is activated and the transmitter system does not include one of the special channel 14 filters, the CH 14 Super precorrection will be outside of the correction range of RTAC. As a result, the transmitter will not pass the FCC mask standard test, will have excessive EVM (error vector magnitude) and a poor EYE pattern.

3.6.2.2 Max Peak Stretch

Peak stretch can cause nuisance overdrive trips in some transmitter models. When the Apex adapts it's non-linearity correction, the algorithm is designed to produce a peak stretch up to a 3 dB limit. Nuisance overdrive trips can be avoided by programming the maximum peak stretch parameter of the RTAC Setup Screen. The maximum peak stretch is adjustable from 3 to 0 dB in 0.25 dB steps in order to limit the peak stretch that the Apex exciter non-linear correction algorithm imparts to its RF output signal.

If they are going to happen, nuisance overdrive trips will typically occur within 30 minutes to 1 hour after transmitter operation with RTAC is first started. If this happens, perform the following:

1 Reduce the peak stretch from 3 dB to 2.5 dB.

2 Wait for one hour to see if further overdrive trips occur.

  A If they do, reduce the peak stretch by another 0.5 dB.

3 Repeat step 2 until overdrive trips cease.

4 Excessive peak stretch reduction may effect the linearity correction of the transmitter.

  A After peak stretch has been adjusted, observe the adjacent channel response to ensure that they still exceed the FCC mask requirements.

3.6.2.3 RTAC Off Air Mode

An RTAC Off-Air Mode parameter gives the customer the option of having the exciter's correction in the hold or bypass mode when the exciter is off line. In bypass mode RTAC settings are discarded when exciter is off line and RTAC must re-adapt when the exciter is switched back on line. In the hold mode, the current correction is stored when the exciter goes off line and is used as a starting point for RTAC when it goes back on line.

WARNING: Disconnect primary power prior to servicing.

3.6.3 Display Setup Screen

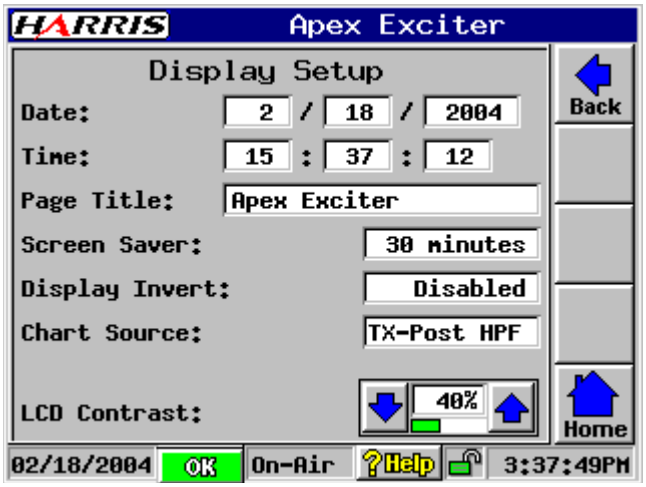

Figure 3-31 Display Setup Screen

The following ia a list of entries on the System setup screen.

- Date: Enter the current date.
- Time: Enter the correct time.

  The exciter will keep track of the date and time, even during periods of power loss, and display the date and time at the bottom of all screens except the Power Up screen.
- Screen Saver: (Range is 1 to 30 minutes) Enter the length of time (on the LCD display numeric key pad) required for the screen to go blank if it is not used.
- Display Invert: When the Display Invert box is pressed, a sub window appears. Pressing Done in the sub window causes the display to be inverted if Enabled is showing and to be upright if Disabled is showing.
- Chart Source: Determines source of Main screen spectrum response display. Choices are:

  8VSB w/RTAC: Digital signal taken at output of adaptive precorrector board.

  8VSB Ref: Digital signal obtained at the output of the modulator board.

  BIT: Digital signal obtained at interface of modulator and adaptive precorrector boards.

  Exciter: RF signal is taken from J4 sample output of exciter PA and connected to J4 sample input on down converter board.

  IPA: From rear panel RF sample input labeled IPA Sample.

  Tx-Pre HPF: From rear panel RF sample input labeled PA Sample.

  Tx-Post HPF: From rear panel RF sample input labeled HPF Sample.

  C, D, and J represent memories on the Adaptive Precorrector board.
- LCD Contrast: A 100% setting gives a bright but washed out screen that is still readable. A 0% setting gives a dark screen of relatively low contrast that is still readable. Enter the desired percent on the LCD display numeric key pad.

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3.6.4 External I/O Setup Screen

Some functions of the APEX digital exciter must be capable of being controlled (operated) via a parallel remote control system while other functions must be controllable from the transmitter logic. The External I/O board is the interface between the APEX exciter and the transmitter control logic.

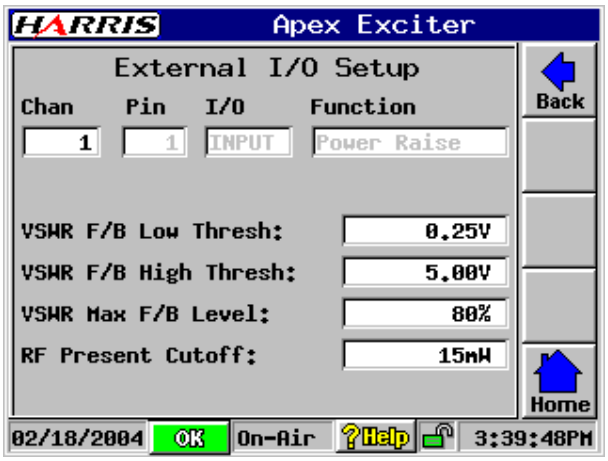

Figure 3-32 External I/O Setup Screen

3.6.4.1 VSWR Foldback Parameters

In some transmitters, such as the Diamond and Platinum, the VSWR foldback threshold is determined by the transmitter control logic, and the actual power level reduction is accomplished by circuits within the exciter. The controller's dc output voltage (to the exciter) has a minimum level, which represents the start of foldback, and a maximum level which represents maximum foldback. The maximum foldback voltage level is expected to reduce the exciter output power to a given minimum, such as 30% of its normal power. A typical range of foldback output voltage from the controller is 0.25 to 5.0 Vdc.

The External I/O Setup screen is shown in Figure 3-32. This screen includes a VSWR foldback function which has three programmable parameters which are listed below.

- VSWR F/B Low Threshold. This represents the input voltage level where the reduction of exciter output power starts. The minimum setting is 0.25 Vdc.
- VSWR F/B High Threshold. This represents the highest input voltage level, which causes the maximum exciter output power reduction.

  The VSWR F/B input voltage causes a linear reduction of exciter output power from the normal exciter output power level (VSWR F/B input voltage below the low threshold) down to the preset maximum allowable exciter output power reduction (when the VSWR F/B input voltage reaches the high threshold).
- VSWR Max F/B Level. This is the maximum allowable exciter output power reduction, listed as a percent of the normal exciter output power, when the VSWR foldback input voltage to the exciter reaches the VSWR F/B High Threshold.

When VSWR foldback is active the following indications will be present.

- The system control light on the front panel will be lighted yellow.
- The foldback readout on the External I/O status screen will be yellow, see Figure 3-21, on page 3-22.

WARNING: Disconnect primary power prior to servicing.

3.6.4.2 RF Present Cutoff

Another programmable function listed in the External I/O Setup screen, shown in Figure 3-32, is the RF Present Cutoff. When the exciter average output power drops to this level, the RF Present (output) signal from the exciter changes from low (exciter is ok) to high (exciter has failed due to low output power). This signal is sent to the transmitter control logic to cause it to switch to the other exciter. The RF present cutoff parameter is programmable from 0 to 250 mW average exciter output power, with a typical setting of half of the normal exciter output power.

3.6.4.3 UHF and VHF Versions of External I/O

Two versions of the External I/O board are available. One for interface with UHF transmitters and one for interface with VHF transmitters. In the Exciter Setup screen, the choice of transmitter effects the type of external interface board used and how it is programmed. Table 3-3 should help explain the options.

A parameter on the External I/O Setup screen is labeled Pin. It displays the connector pin number for the associated channel number of the External I/O board. I/O lines are still indexed using the channel number.

Table 3-3 Transmitter Choice Verses Type of External Interface Board

Transmitter Choice	Type of Board	Channel Programming	Channel to J1 Assignments
Platinum CD (Harris)	VHF	Fixed	See Note 2. for all four transmitter choices.
Sigma CD (Harris)	UHF	Fixed	
Diamond CD (Harris)	UHF	Fixed	
Ranger (Harris)	UHF	Fixed	
PowerCD (Harris)			
Custom (Other DTV Tx.)	VHF or UHF	See Note 1.	
Note 1. Each channel can be programmed according to requirements of transmitter.			
Note 2. Channel to J1 pin assignment is fixed for VHF (Tables 3-5 and 3-6) and UHF boards (Tables 3-4 and 3-6).			

In the Custom Transmitter mode, channels 1 through 18 can be individually selected and programmed. Refer to Table 3-6 for J1 Pin assignments and their corresponding channels. The programming choices for each channel are as follows.

The choices are Status Input or Status Output.

- The voltage high level is 4.0 Vdc, and the voltage low level is 1.0 Vdc.
- A status input can sink 5 mA and a status output can sink 20 mA.
- The absolute maximum range is -0.3 to +15 Vdc.

The function choices are as follows.

- Power Raise (input) RF output power is raised when input pulled low
- Power Lower (input) RF output power is lowered when input pulled low
- Mute Command (input) Will mute exciter when input pulled low
- Mute Status (output) This output is low when the exciter is muted
- RF Present (output) Output is low if exciter RF output level is above a given level. The RF present cutoff parameter is programmable from 0 to 250 mW.

- Eq Hold (input) The RTAC Equalizer is put on hold when input pulled low
- Exciter Active (input) This is a status input from the exciter switcher controller. It is high when this exciter is on the air.
- Eq Reset (input) This function shares the same input terminal at the Exciter Active input. The RTAC Equalizer will be in hold or bypass (depending on setting of RTAC Off-Air Mode, see Section 3.6.2, RTAC Setup Screen on page 3-32) when input pulled low and the exciter is not on the air.
- TS Loss (output) This output is low when transport stream is lost.
- Unused (input or output)

The analog inputs and outputs are not programmable in Custom Transmitter mode. Their function is fixed by the type of External I/O board (VHF or UHF).

3.6.4.4 UHF External I/O

A list of entries on the UHF External I/O setup screen is shown in Table 3-4. This table also lists connector J1 pin assignments, corresponding channel numbers, and the function (input or output, and its description).

Table 3-4 UHF External I/O Parallel Control Interface Connector J1(25 pin male)

J1 Pin Number	Input/Output and Channel No.		Description
1	Status Input	1	Power Raise
2	Status Input	3	Power Lower
3	Analog Input 3		No Connection
4	Analog Output 1		No Connection
5		5	No Connection
6	Status Input	7	Mute Command
7		9	No Connection
8	Status Output	11	Mute Status
9		13	No Connection
10	Status Input	14	Equalizer Reset (input grounded) and Enable (Exciter Active) Command (input open or high)
11	Status Input	15	Equalizer Hold
12	Analog Input 1		VSWR Fold back (dc voltage sample)
13	Analog Input 2		No Connection
14		2	No Connection
15	Status Output	4	Exciter RF Presences Status
16	Analog Input 4		No Connection
17	Analog Output 2		No Connection
18		6	No Connection
19		8	No Connection
20	Status Input	10	Spare Input
21	Status Output	12	Spare Output
22 - 25			Ground

3.6.4.5 VHF External I/O

The following ia a list of entries on the VHF External I/O setup screen. Refer to Table 3-5 for a list of connector J1 pin assignments, the corresponding channel numbers, and the function (input or output, and its description).

Table 3-5 VHF External I/O Parallel Control Interface Connector J1(37 pin female)

J1 Pin Number	Input/Output and Channel No.		Description
1	Status Input	1	Power Raise
2	Status Input	3	Power Lower
3		6	No Connection
4		8	No Connection
5		9	No Connection
6	Status Input	7	Mute Command
7	Analog Output 1		Power Sense
8	Analog Output 2		No Connection
9	Status Output	11	Mute Status
10		13	No Connection
11	Status Output	4	Phase Lock Loop Status
12		17	No Connection
13		5	No Connection
14	11.5 Vdc		+11.5 Vdc Source
15	Analog Input 1		VSWR Fold back (dc voltage sample)
16	Analog Input 2		No Connection
17		2	No Connection
18	Status Input	14	Equalizer Reset (input grounded) and Enable (Exciter Active) Command (input open or high)
19	Status Input	15	Equalizer Hold
20		10	No Connection
21		12	No Connection
22		16	No Connection
23			Ground
24			Ground
25			Ground
26			Ground
27 - 37			No Connection

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Table 3-6 Channel Number to J1 Pin Number

Custom Channel to J1 Pin Channel Relationship			Custom Channel to J1 Pin Channel Relationship		
Channel No. (on screen)	**VHF Board J1 Pin Number**	**UHF Board J1 Pin Number**	**Channel No. (on screen)**	**VHF Board J1 Pin Number**	**UHF Board J1 Pin Number**
1	1	1	Analog In 1	15	12
2	17	14	Analog In 2	16	13
3	2	2	Analog In 3		3
4	11	15	Analog In 4		16
5	13	5			
6	3	18	Analog Out 1	7	4
7	6	6	Analog Out 2	8	17
8	4	19			
9	5	7	Ground	23 - 26	22 - 25
10	20	20			
11	9	8	No Connect	27 - 37	
12	21	21			
13	10	9	11.5 Vdc Out	14	
14	18	10			
15	19	11			
16	22				
17	12				

3.6.5 Serial I/O Setup Screens

The Serial I/O entry of the System Setup screen has three sub screens associated with it. They are as follows:

- Serial Setup 1/3, RS-232
- Serial Setup 2/3, Ethernet
- Serial Setup 3/3. CAN (bus)

3.6.5.1 Serial Setup Screen 1 of 3, RS-232

The purpose of the Serial Setup screen is to program the serial ports on the front and rear panel of the exciter.

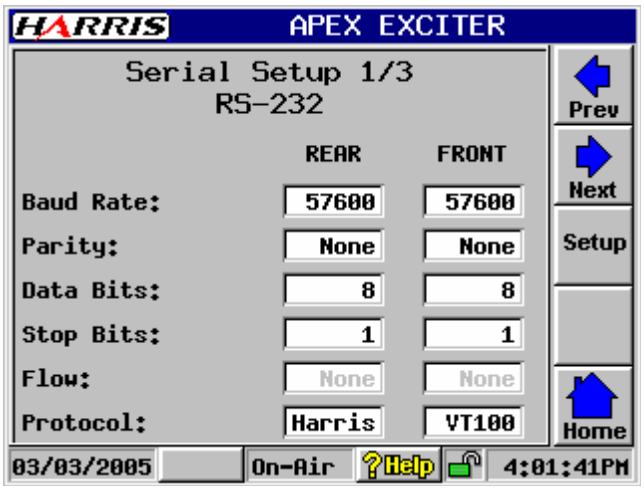

Figure 3-33 Serial Setup Screen 1 of 3, RS-232

Since the setup parameters for the front and rear connectors are the same, only one set will be described. The following ia a list of entries on the Serial setup screen.

- Baud: Enter the baud rate on the touch screen numeric key pad. Baud rate choices are 300, 600, 1200, 2400, 4800, 9600, 19.2k, 28.8k, 38.4k, 57.6k, and 115.2k.
- Parity: Choices are None, Odd, or Even.
- Data Bits: Choices are 7 or 8.
- Stop Bits: Choices are 1 or 2.
- Flow: This entry is fixed at None.
- Protocol: Selections are VT100, Harris.

The Harris protocol is used for software upgrades, see Section 5.2, Loading Software on page 5-11.

The VT100 protocol is rarely used.

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3.6.5.2 Serial Setup Screen 2 of 3, Ethernet

This screen is for programming the LAN 10 Base-T Ethernet port on the rear panel of the exciter.

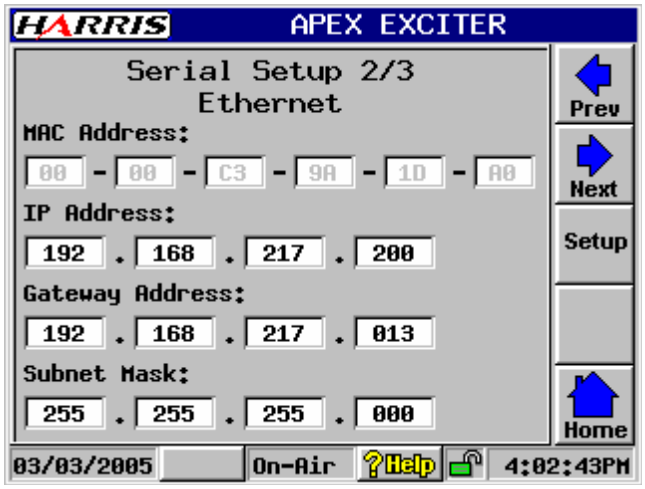

Figure 3-34 Serial Setup Screen 2 of 3, Ethernet

At the present time the ethernet port is set to talk to the eCDi™, which is a transmitter network interface unit. The APEX exciter software must be version 4.0 or later to activate the ethernet port for use with eCDi. See the APEX Exciter Setup and the Setting APEX IP Address sections of the eCDi technical manual (part number 888-2517-001) for detailed instructions.

The IP address must be correct for the exciter to communicate with the eCDi.
The IP addresses for eCDi units with software revisions of 2.6 or later are as follows.

- For exciter A the IP address is 192.168.217.200
- For exciter B the IP address is 192.168.217.201

The IP addresses for eCDi units with software revisions earlier than 2.6 are as follows.

- For exciter A the IP address is 192.168.0.200
- For exciter B the IP address is 192.168.0.201

The gateway address is unimportant when exciter is used with the PowerCD transmitter.

The Subnet Mask can remain at 255.255.255.0.

The MAC address is unique for each exciter and has been assigned to it during final test. This number will stay with the exciter during software changes. The MAC address, along with all user setups are stored in the controller board. If the controller board is changed in the field, the user setups and the MAC address must be reentered. If lost, the MAC address may be obtained from Harris, provided the exciter serial number is known.

The MAC address is greyed out (locked) because the Setup Screen > Factory Setup window is locked.

> To obtain the MAC address for a given exciter or to reenter the MAC address into an exciter, contact Harris technical support. The serial number of the exciter must be known in order to obtain the MAC address from Harris.

3.6.5.3 Serial Setup Screen 3 of 3, CAN

This screen is for programming the CAN connector on the rear panel of the exciter. This window became available with APEX exciter software versions 5.2 and later.

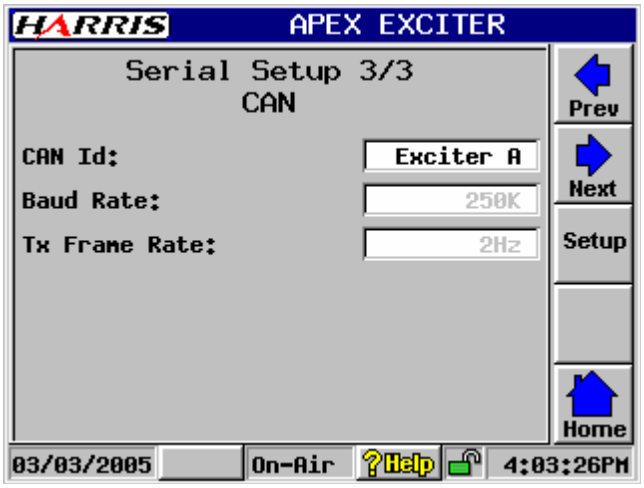

Figure 3-35 Serial Setup Screen 3 of 3, CAN

The exciter CAN bus is used with the PowerCD transmitter and with some earlier Diamond and SigmaCD transmitters.

- The CAN ID is selectable between Exciter A and Exciter B.
- The Baud Rate is as follows:

  Default is 125 kHz

  Rate for Diamond and SigmaCD transmitters is 133 kHz

  Rate for PowerCD transmitter is 250kHz.

- The Tx Frame Rate is as follows:

  Default is 1Hz

  Rate for PowerCD, Diamond and SigmaCD transmitters is 2 Hz.

Improper Baud or Tx Frame rates will lock up the CAN bus. The solution to this problem is to set the rates correctly, or in the case of Diamond or SigmaCD transmitters the CAN cable may be unplugged form its connector on the rear of the exciter. The exciter CAN bus cables have been removed on current productions of Diamond and SigmaCD transmitters.

The Baud and Tx Frame rate windows are normally greyed out (locked). To unlock these windows and set the two rates perform the following.

1 Go to the Home > Setup > Exciter > Transmitter select window and set the selection to Custom, then click done.

2 Return to the Serial Setup 3/3 CAN screen (Home > Setup > Serial I/O > Serial Setup 3/3 CAN) and change the two rates.

   A Click in the appropriate window, use the up or down arrows to select the correct rate, then click on Done.

3 Return to the Home > Setup > Exciter > Transmitter window and set the correct transmitter choice, then click done.

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3.6.6 Change Passwords > Security Setup

Figure 3-36 Security Setup Screen

Two passwords can be entered in the change passwords > security setup screen, refer to Figure 3-36. They are:

- User Password: This password is needed to unlock the User Setup entry on the System Setup screen (shown in Figure 3-37, on page 3-44), if it is locked.
- Diagnostics Password: This password is needed to unlock the Diagnostics Setup entry on the System Setup screen (shown in Figure 3-37, on page 3-44), if it is locked.

  The channel select and pilot frequency offset entries on the exciter setup screen are locked when the diagnostics setup is locked.

If either password change screen is entered, an alpha/numeric touch keypad is displayed with the current password is shown at the top. To change a password:

1 Use the keypad to type a new password.

  A The password is case sensitive. The password must be entered with the correct case to unlock a function.

  B Spaces can be used as part of a password.

  C If spaces are used at the end of the password, or one or more spaces are used entirely as a password, they will not show up when the System Setup > Change Password screen is entered, but they must be correctly entered to unlock that function.

2 When the new password is entered, it can be accepted by pressing Done, or the old password can be retained by pressing Cancel.

WARNING: Disconnect primary power prior to servicing.

3.6.6.1 User Setup (Locked or Unlocked)

If the User Setup is locked, all setup functions and the exciter power raise and lower functions will be locked and their various setup screen selection values will be greyed out. Only the Exciter Setup screen Channel and Frequency Offset functions will be available.

In the System Setup screen, see Figure 3-37, pressing the box to the right of User Setup pulls up a Security window with the statement “User Setup will be Locked”. The choices are Ok or Cancel.

- If Cancel is selected, the User Setup functions will remain unlocked.
- If Ok is selected, the user setup functions will be locked.

To gain access to the setup functions, the System Setup > User Setup: Locked screen must be entered. This time an alpha/numeric keypad will appear.

- Enter the correct password and select Done.

  If the password is correct, User Setup will change to Unlocked, if incorrect it will remain locked.

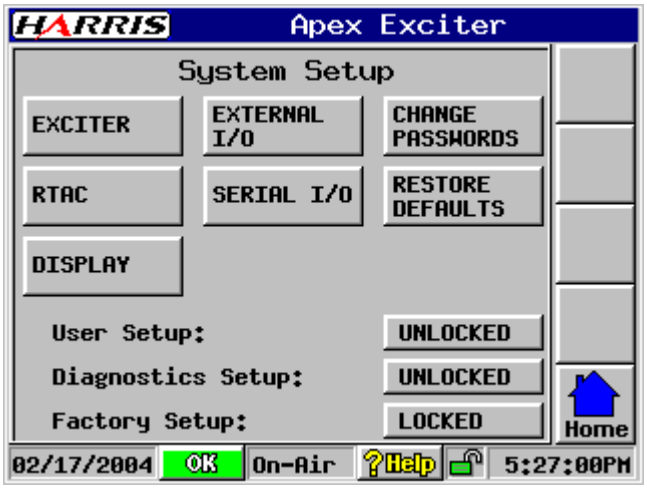

Figure 3-37 System Setup Screen

3.6.6.2 Diagnostics Setup (Locked or Unlocked)

If the Diagnostics Setup is locked, all diagnostics functions and the Exciter Setup screen Channel and Frequency Offset functions will be locked, and their various diagnostics screen selection values will be greyed out.

In the System Setup screen, see Figure 3-37, pressing the box to the right of Diagnostics Setup pulls up a Security window with the statement “Diagnostics Setup will be Locked”. The choices are Ok or Cancel.

- If Cancel is selected, the diagnostics functions will remain unlocked.
- If Ok is selected, Diagnostics Setup will be locked.

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To gain access to the diagnostics and channel change functions, and the channel and frequency offset select entries on the exciter setup screen, the System Setup > Diagnostics Setup: Locked screen must be entered. This time an alpha/numeric keypad will appear.

- Enter the correct password and select Done.

  If the password is correct, Diagnostics Setup will change to Unlocked, if incorrect it will remain locked.

  Diagnostics functions can now be used, and these functions will be remain available until the Diagnostics Setup screen status is changed to Locked.

3.6.6.3 Factory Setup (Locked or Unlocked)

The Factory Setup in the System Setup screen, see Figure 3-37, on page 3-44, is normally locked. It is not a customer feature. If the System Setup > Factory Setup: Locked soft key is pressed, an alpha/numeric keypad will appear. A password is required unlock this function. This feature locks several functions that are accessed in the factory when the unit is being tested.

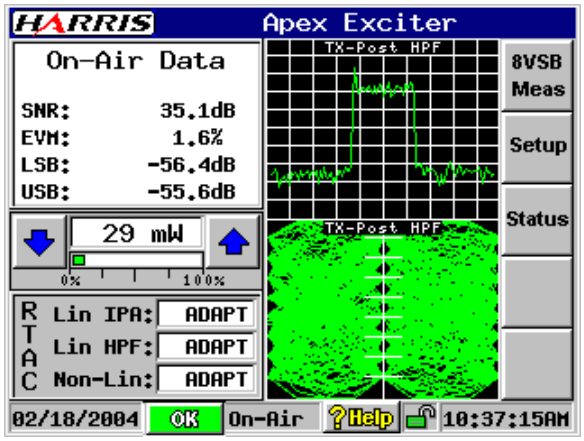
3.6.7 Restore Defaults

The restore defaults soft key on the System Setup screen, see Figure 3-37, on page 3-44, is locked under the Factory Setup password.

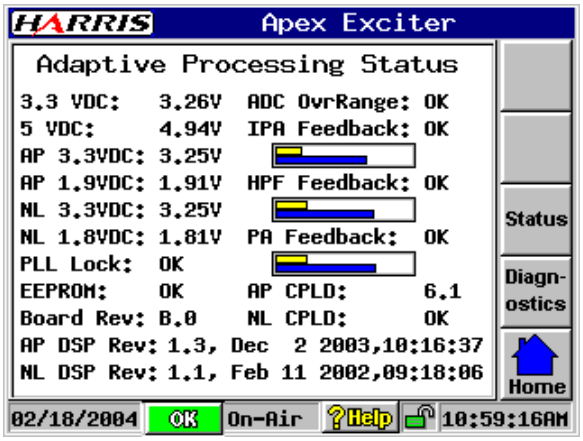
WARNING: Disconnect primary power prior to servicing.

3.7 RTAC Operating Procedures

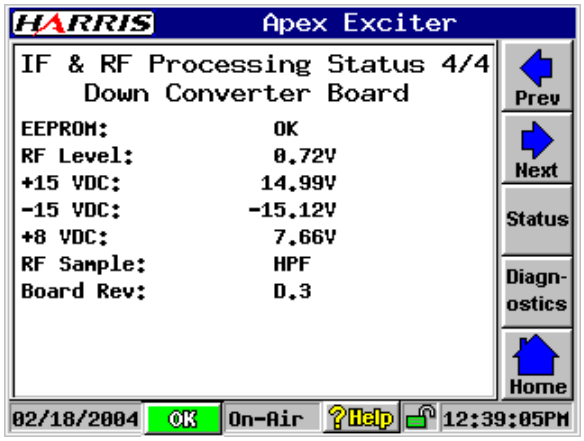
RTAC operation involves several exciter screens. The operating information is summarized below. For convenience, the screen shots are reproduced in Figure 3-38.



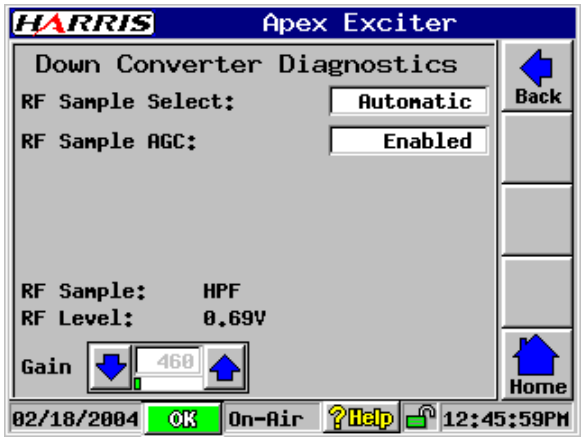
Main Screen



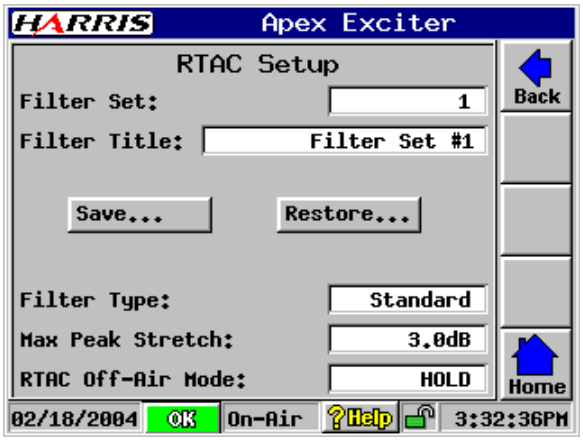
Adaptive Processing Status Screen



Down Converter Status Screen



Down Converter (Status) Diagnostics Screen



RTAC Setup Screen

Figure 3-38 Five Screens Needed for RTAC Operation

WARNING: Disconnect primary power prior to servicing.

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3.7.1 From RTAC Section of Main Screen

Refer to Figure 3-38. The various sections of RTAC correction which can be activated from the main screen are:

- Lin IPA (IPA RF feedback sample)
- Lin HPF (RF feedback sample taken after the high power filter)
- Non-Lin (PA output feedback sample, taken before the high power filter).

The possible states for each corrector are:

- Bypass: Turns the selected corrector off
- Default: Selects a pre loaded correction algorithm from the RTAC Filter Setup screen. Saving an RTAC correction algorithm to an RTAC filter is covered in Section 3.6.2 on page 3-32.
- Adapt: Turns the selected corrector on
- Hold: Keeps the last correction value for the selected mode. This is a short term option. For long term use select Default.

If any of the three choices above is set to Adapt and its RF sample to the down converter board is missing or is outside the prescribed input power range, the adaptation for that choice will not be performed. In either of the above two failure modes, that RF sample, shown in the adaptive precorrection board status screen, will show fault.

3.7.2 From Adaptive Precorrection Board Status Screen

Refer to Figure 3-38. Each of the three RF sample feedbacks below has a bar graph on the adaptive precorrection board status screen. The yellow (upper) bar indicates average power level and the blue (lower) bar indicates peak level. The RF input sample is within the correct power range (-10 to 0 dBm) when both bars are within the center range of the window. The bar graphs show the signal level at the output of the sample AGC circuit. If any input sample is outside the allowable power range, the bars for that input will be at an extreme end of the widow and that input will be faulted.

If one or more RF samples to the ADC exceeds maximum allowable level the ADC Over Range indication on the adaptive precorrection board status screen will be faulted.

Note

Maximum input level for the three feedbacks mentioned above should not exceed +5 dBm. Excessive input levels (+20 dBm or greater) will cause faults for the ADC and feedback inputs and can also cause crosstalk between inputs and/or damage to the exciter.

3.7.3 From Down Converter Board Status Screen

Refer to Figure 3-38. Two entries on the IF &RF Processing Status > Down Converter Status screen are of interest to RTAC operation, They are:

- RF Sample: This indicates which down converter sample is currently active.
- RF Level: RF level (taken after the AGC circuit) for the current sample. It typically ranges between 0.5 to 1.0 Vdc for samples of proper input power range.

If known good samples are present at the exciter inputs, and they are not all being sampled, or their level is wrong, the down converter diagnostics screen should be checked.

WARNING: Disconnect primary power prior to servicing.

3.7.4 From Down Converter Diagnostics Screen

- RF Sample Select: (Automatic, Exciter, IPA, Amplifier, or HPF).

  When Automatic (normal mode) is selected, the controller board causes the down converter to switch between the IPA, Amplifier, and HPF inputs. The exciter is only sampled when the Setup > Display > Chart Source is set to monitor the exciter.

  When not in automatic mode, the down converter is locked to the Exciter, IPA, Amplifier, or HPF sample input.

- RF Sample AGC: (Enabled or Disabled), enabled mode is normal.

  When enabled is selected, the level of each RF sample (at the output of the down converter) is adjusted to the correct level for the ADC (analog to digital converter).

  When disabled, for test purposes, the level of each RF sample must be manually set by the blue up and down gain arrows at the bottom of the screen. The possible range is 0 to 4096.

- RF Sample tells which sample input to the down converter is currently active.
- RF Level: This is the current RF sample level (taken after the AGC circuit). It typically ranges between 0.5 to 1.0 Vdc when the input sample is within proper power range.
- Gain: This control is only active when RF Sample AGC (on this screen) is defeated. It is used to set the down converter gain so that the sample level falls between 0.6 and 1.0 Vdc.

3.7.5 From RTAC Setup Screen

Up to four Existing RTAC correction setups can be saved. An option to name each saved filter setup exists. Filter setups can be stored for many reasons, such as when the transmitter was first installed, after transmitter maintenance, and etc. They are good for comparative testing of the transmitter and RTAC correction.

- Filter Set: (selections include 1 through 4)
- Filter Title: Brings up an alpha/numeric touch keypad to enter the name for the selected filter set.
- Save: Pressing this soft key saves the current RTAC setup to the filter set selected.

  The filter set should be given a name (in the filter title selection).

- Restore: Applies the selected, pre-saved filter set to the RTAC correction algorithm. This causes the Main screen RTAC samples to be set to Default, which applies the pre-saved filter set to the RTAC correction algorithm.

See Section 3.6.2, RTAC Setup Screen on page 3-32 for RTAC setup instruction.

4 APEX™ Exciter Theory of Operation

4.1 General Description

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The program input to the exciter is a data signal called the “Transport Stream” which is coded in the SMPTE 310M format and has an impedance of 75 ohms. This form of coding allows the clock signal to be recovered from the data stream, instead of requiring separate clock and data paths.

The exciter processes this input into the on-channel 8VSB transmission signal needed as drive for the transmitter power amplifiers. RTAC™ (Real Time Adaptive Correction) correction circuits in the exciter predistort the exciter RF output to compensate for errors which occur in the power amplifiers and the high level RF output intermod filter. The purpose of the correction circuits is to produce a transmitter output signal with good EVM (error vector magnitude), good signal to noise ratio, and very low intermodulation (adjacent channel) products. RTAC™ processing in the digital part of the exciter continually monitors and trims exciter linear and nonlinear correction to maintain top performance.

Control and monitoring of the exciter is provided by a front panel display and remote control connection, and, in some transmitters exciter control is also extended to the transmitter control cabinet GUI (graphical user interface) display.

The APEX™ exciter performs the following general functions:

- SMPTE310M Input & Clock Distribution
- Data synchronization
- Channel encoding
- Sync and pilot insertion
- Pre-correction
- Nyquist filtering (spectral shaping)
- Up conversion
- RTAC™ (Real Time Adaptive Correction)

The on-channel 8VSB RF signal is output through a 50-ohm SMA connector at the rear of the exciter. This output signal is suitable for amplification in subsequent high-power stages.

4.2 Transmitter Systems Block Diagram

Figure 4-1 is a block diagram which shows a DTV transmitter with an APEX exciter. This diagram shows the transport stream input to the exciter, the exciter RF output signal connected to the transmitter IPA input, and the various required RF feedback signals from the transmitter system to the exciter. These feedback signals are needed to perform the linear and non-linear RTAC precorrection of exciter RF output signal.

The information contained in this overall system block diagram will be needed later, when a detailed study of the APEX exciter block diagram is provided.

Additional exciter to transmitter systems interconnection information is covered in Section 2, APEX Exciter Installation.

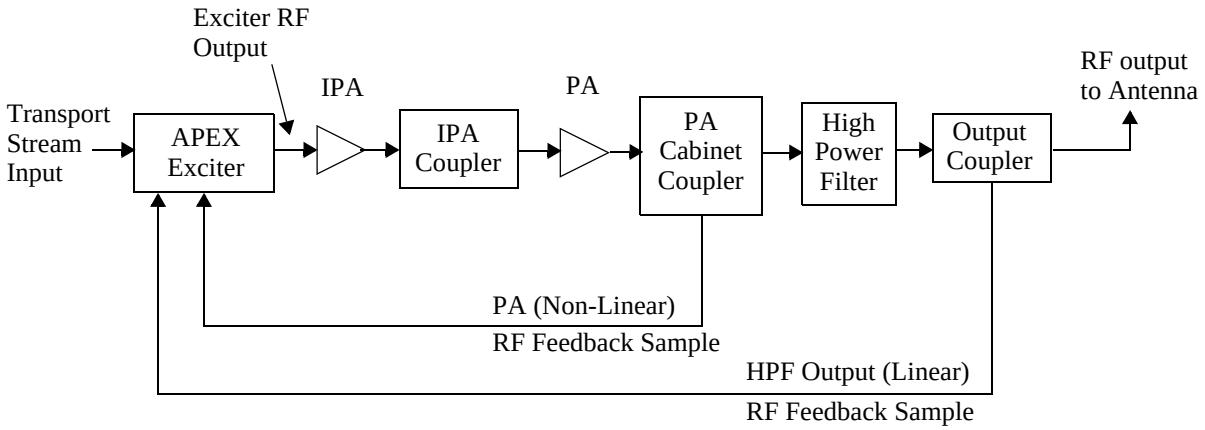

Figure 4-1 APEX Exciter/ Transmitter - RF Interconnection Block Diagram

4.3 APEX Exciter Digital Assembly Overview

Figure 4-3 is an overall block diagram of the APEX exciter. Refer to it while studying the exciter digital assembly, also, refer to Figure 5-2, on page 5-3 for a view of the physical layout digital tray.

The APEX exciter digital assembly (bottom side of exciter) accepts dc supply voltages from the power supply board (located in the top, analog side of the exciter) and a DTV transport stream as input. This tray provides a fully modulated 8VSB first IF output centered at 10.76 MHz.

The digital assembly also performs RTAC™ (real time adaptive correction) pre-correction on the signal following the modulation and spectral filtering processes. Three down converted samples from various locations along the transmitter system are compared the output of the modulator board to shape the pre-corrected RF output signal of the exciter. This pre-corrected signal minimizes the nonlinear and linear distortions of PA and high power filter.

The digital assembly consists of 7 circuit boards:

- A14 - SMPTE 310 board
- A13 - Modulator board
- A9 - Adaptive Precorrection board
- A12 - DAC (digital to analog converter) board
- A11 - ADC (analog to digital converter) board
- A8 - Controller Board
- A7 - External I/O (input/output) Board

Signal flow from input to output of the digital (bottom) assembly of the exciter may be followed by referring to Figure 4-3. The transport stream is input to the SMPTE 310 board, A14, where the transport stream data and the clock are recovered from the SMPTE310M signal. This board uses the recovered transport stream clock to phase lock a 43.048 MHz

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oscillator. This signal is the 43.048 MHz clock, required by several boards in the digital assembly. The 43.048 MHz clock is divided by four to produce the 10.762 MHz clock required by the first local oscillator in the PLL board of the analog assembly.

From A14, the signal progresses to A13, the modulator board, where randomization, Reed-Solomon coding, and trellis coding occur and segment sync and frame sync are added. The signal is also band-limited using a root-raised cosine filter.

The modulator board output passes through the controller board (A8) and on to the adaptive precorrector board (A9).

The adaptive precorrector board performs both linear (response and group delay) and non-linear (phase and linearity) RTAC™ pre-correction on the signal as the symbol stream passes through it. RTAC pre-correction is performed as follows.

The ADC (A11) receives the transmitter feedback samples from down converter board (A5) of the analog assembly and converts it to the same digital format as the signal from the modulator board. The modulator board output and the feedback samples are then compared in the adaptive precorrector board and adjustments are made to pre-correct the output signal of the adaptive precorrector board. The pre-corrected signal cancels the non-linear and linear distortions generated by the transmitter system PA and high power filter.

The adaptive precorrector board output is applied to the DAC board (A12), which converts the 43.048 Mega-Sample/second digital stream to the 10.762 MHz (center frequency) analog first IF output, which is sent to the up converter board (A3) of the analog assembly.

4.3.1 Controller Board Theory

The controller board controls all of the other boards except the power supply and the fan. It indirectly controls the output amplifier through the APC (automatic power control) and the mute function.

A built in communication engine handles all communications independent of CPU core.

Some of the controller board functions include the following.

1 Boot loads micro processor (itself) from flash.

   A Copies application from flash to SDRAM (synchronous dynamic random access memory). The application runs from SDRAM.

2 Does CRC (cyclic redundancy check)

3 Microprocessor boot loads other exciter sub systems, getting information from flash.

   A Accesses CPLD version via CPLD JTAG. If CPLD version matches, it goes on to rest of system. If it does not match, it programs the CPLD.

   B It loads External I/O, Adaptive Precorrector, Modulator, SMPTE-310, Front Panel, and UDC Interface Boards

4 Continually checks all external interfaces, which include:

- External I/O board, which includes the CAN bus, digital I/O (parallel exciter control and status), analog I/O (such as VSWR fold back)
- 10 Base T (Ethernet port)
- RS232 ports, front and rear panels
- 1/4 color VGA (touch screen)
- UDC Interface board.

WARNING: Disconnect primary power prior to servicing.

The adaptive precorrector and modulator boards are autonomous following boot loads, with periodic health checks from the controller board.

The HPI (host port interface) and SPI (serial peripheral interconnect) are the means of communication between the controller board and the adaptive precorrector and modulator boards.

4.3.2 RTAC and Adaptive Precorrector Board Theory

Adaptive precorrection is a process where an RF sample from somewhere along the transmitter system is down converted to the 1st IF frequency in the down converter board, converted to a digital signal in the ADC board, and the digitized sample is sent to the adaptive precorrector board where it is time aligned with and compared to the reference digital signal from the modulator board. The results of this comparison are used to pre correct the digital output signal from the adaptive precorrector board so that it will cancel certain distortions generated in the transmitter system power amplifiers and high power filter (HPF).

Adaptive precorrection is divided into two general areas.

- Non linear correction: This refers to amplifier non linearity, which is poor linearity (also referred to as AM to AM conversion) and ICPM (incidental carrier phase modulation), also referred to as AM to PM conversion.

  Non linear distortion causes intermodulation products to appear in the adjacent channels, making it difficult or impossible for the transmitter to pass the FCC response mask test without some type of amplifier linearization.
- Linear correction: This generally refers to filter, tuned circuit, or coupling circuit distortions, which are amplitude response problems and group delay (also called PM to PM conversion).

  Linear distortions cause the eyes in the 8VSB eye pattern to close. This increases EVM (error vector magnitude) and degrades the transmitter signal to noise performance.

The RTAC correction circuits perform their operations in several sequential steps, which are as follows.

- The IPA feedback signal is used by RTAC to correct linear distortions generated by the transmitter system in the IPA and previous circuits. Since the IPA is expected to be a very linear amplifier, this provides a near perfect drive signal for the PA.
- The PA feedback signal is used by RTAC to correct non linear distortions generated by the transmitter PA. This provides a near perfect input signal for the high power filter.
- The HPF feedback signal is used by RTAC to correct linear distortions generated by the transmitter high power filter, and the smaller amounts of linear distortions caused by tunable PAs.

The adaptive precorrection board is also capable of pre distorting the transmitter output signal to correct for group delay caused by wave guide when it is used to transport the transmitter RF output signal to the antenna. The waveguide type and length are entered in exciter setup screen. Since waveguide group delay correction predistorts the transmitter output signal, the EVM performance and EYE pattern appearance of the transmitter output signal will appear poor. The waveguide precorrection is subtracted out of the exciter main screen EYE pattern and on-air data, so they will reflect the condition of the transmitter.

4.3.2.1 Special RTAC Precorrection For Channel 14 HPFs

Channel 14 digital transmitters may interfere with some land mobile radio systems even though the transmitter passes the FCC mask standard. These transmitter require a special HPF (high power filter) to protect land mobile radio operators who are operating immediately below channel 14, some as close as 25 kHz from the lower channel 14 limit. The required attenuation for these filters ranges form 40 to 70 dB. Typical configurations include 12 to 18 pole elliptical filters which may or may not include discrete separate notch filters. These filters may be single ended or balanced (constant impedance filters). Due to the high Q, rapid response rolloff and deep attenuation required, these filters produce large amounts of group delay and response changes at the lower end of the channel. Pilot attenuation may be as high as 1.5 dB, and group delay at the lower edge of the channel may be as much as 2000 nanoseconds. Precorrection is required to enable the RTAC (real time adaptive correction) to correct the above mentioned linear distortions caused by these filters.

The Setup > RTAC Setup > Filter Type: CH 14 Super applies the necessary amplitude response and group delay precorrection, which reduces the distortions within the correction range of the RTAC circuits.

Caution

If the CH 14 Super selection is activated and the transmitter system does not include one of the special channel 14 filters, the CH 14 Super precorrection will be outside of the correction range of RTAC. As a result, the transmitter will not pass the FCC mask standard test, will have excessive EVM (error vector magnitude) and a poor EYE pattern.

4.3.3 SMPTE-310M and Clock Distribution

The SMPTE 310M signal enters the exciter at J5, which is the input to the SMPTE 310 Board. This board receives the signal and converts the 310M signal to a more useful form during subsequent processing. The board also uses the embedded clock in 310M to create internal clock signals which are routed to other parts of the exciter.

The SMPTE 310M input connector is an isolated connector. The shield of the cable is not grounded at the exciter input. This allows superior common-mode rejection. An adaptive cable equalizer which corrects for up to 1000 feet of high-quality 75 ohm cable is included in board.

A programmed device uses the recovered clock to restore the data stream from SMPTE 310M format to basic data NRZ format for use in the modulator board. It also searches for the hex 47 sync byte and rechecks for it continually. When three successive “47" sync bytes are found at 188 byte intervals the transport stream is considered locked, and the MPEG Input Status screen SMPTE Input Lock shows OK.

If a sync byte is not seen at the proper interval, lock confidence is lowered. When three successive sync bytes are not seen the MPEG Input Status screen SMPTE Input Lock shows Fault.

A data segment sync pulse is produced every 188 bytes for use elsewhere in the 8VSB modulator.

4.3.3.1 43.048 MHz Phase Lock Loop

A crystal oscillator is used to generate the 43.04 MHz clock signal for the rest of the 8VSB modulator tray. It is phase-locked to the 19.39 MHz transport clock. The 43.04 clock is divided by 4 to produce the 10.76 MHz clock, see Figure 4-2 for a block diagram of the 43.048 MHz phase lock loop.

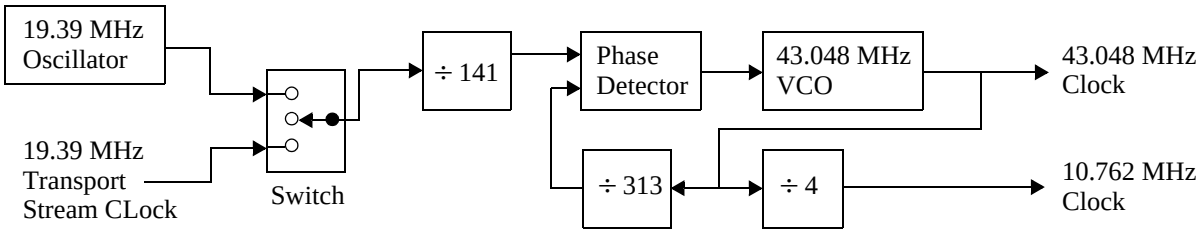

Figure 4-2 The 43.048 MHz Phase Lock Loop

As shown in Figure 4-2:

- The 43.048 MHz VCO is locked to the incoming transport stream clock when the transport stream is present and the exciter setup screen > SMPTE Test Pattern selection is set to off.
- The 43.048 MHz VCO is locked to the 19.39 MHz oscillator when the exciter setup screen > SMPTE Test Pattern selection is set to one of the test patterns.
- The 43.048 MHz VCO is not locked to either 19.39 MHz source when the transport stream is absent and the SMPTE Test Pattern selection is set to off.

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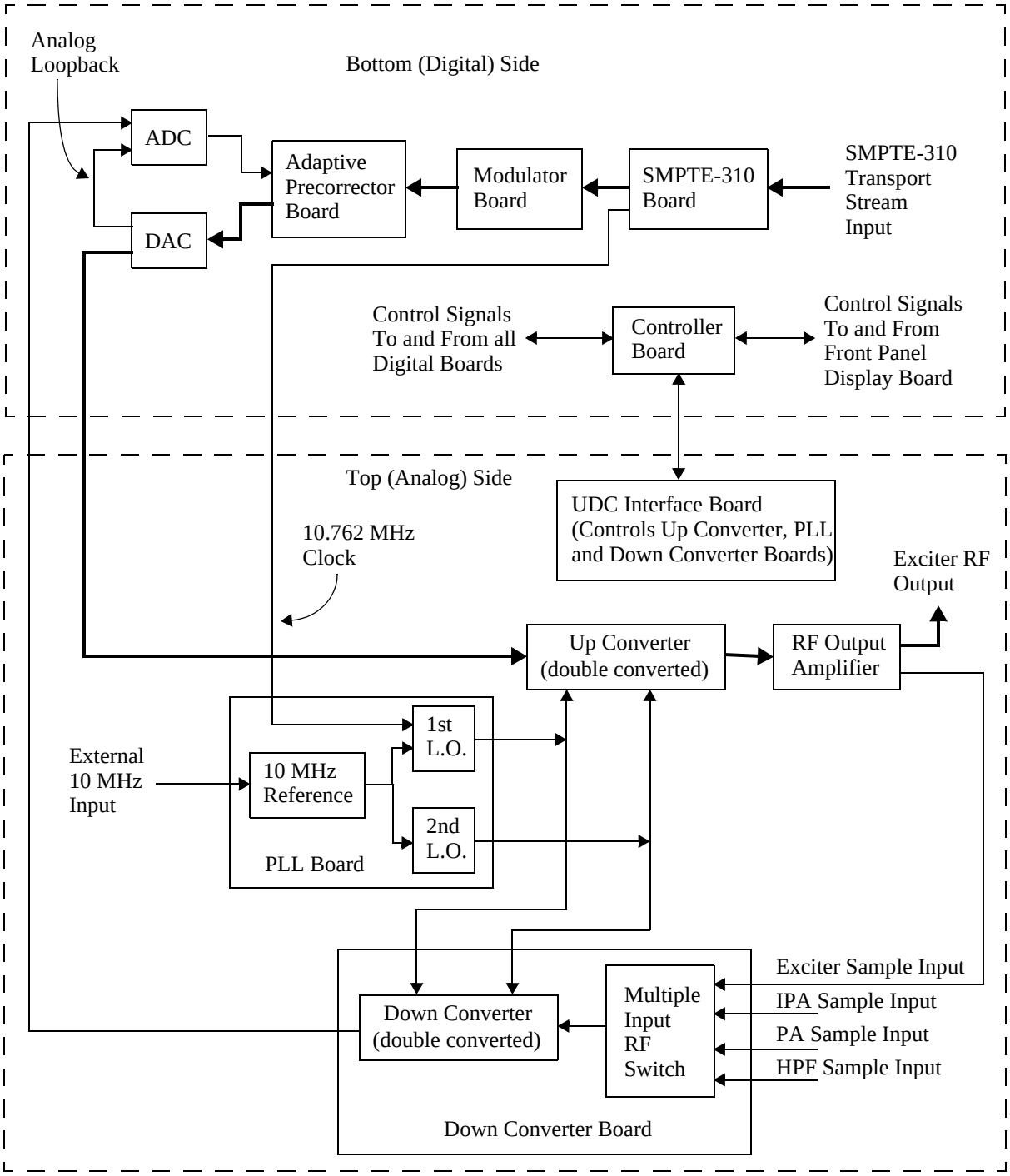

Figure 4-3 APEX Exciter - Signal Flow Block Diagram

WARNING: Disconnect primary power prior to servicing.

4.4 APEX Exciter Analog Assembly Overview

The analog assembly (top side of exciter) contains the following subassemblies. Refer to Figure 5-1, on page 5-2 for a view of the analog (top side) assembly circuit board layout.

- A1 - Exciter power supply board
- B1 - Cooling fan.
- A6 - UDC (up/down converter interface) board
- A4 - PLL (phase lock loop) board
- A3 - Up Converter board
- A2 - Output Amplifier board
- A5 - Down Converter board.

Refer to Figure 4-3 for a block diagram of the APEX exciter.

The up-converter accepts a 10.76 MHz IF from the DAC (digital to analog converter board (A12) connector J3. The up converter converts the signal in two stages to an on channel VHF or UHF output. It may be configured (via the front panel touch screen) to place the exciter output on any VHF or UHF channel.

Local oscillators used for up and down conversions are generated via low noise phase locked loops. All frequencies are referenced to a common 10 MHz standard. An external 10MHz reference input is provided in case precise frequency control of the pilot is needed.

Power output capability of the exciter is 250 mW average power.

The down converter sequentially selects the four RF feedback samples from the transmitter system and converts them down to the 10.762 MHz 1st IF frequency. This signal is sent to the ADC (analog to digital converter) board.

The UDC interface sends commands from the digital assembly controller board to the down converter, PLL, and up converter boards, and receives status signals from them.

4.4.1 Up Converter Board Block Diagram Description

Refer to Figure 4-5 for a simplified block diagram of the up converter.

The up converter receives the 10.762 MHz 1st IF signal from the DAC and heterodynes it up to a 140 MHz 2nd IF frequency. The conversion requires a 129.24 MHz CW signal from the 1st LO (local oscillator) circuit on the PLL board.

The 2nd conversion stage of the up converter heterodynes the 140 MHz 2nd IF signal to the on channel frequency, using a CW signal from the 2nd LO circuit in the PLL board.

The 2nd local oscillator is injected on the high side of the IF signal for the VHF channels and on the low side of the IF signal for the UHF channels. This means that the 10.762 MHz 1st IF spectrum will appear inverted (pilot on the high side of the signal) for VHF operation and will appear normal (pilot on the low side of thee signal) for UHF operation, as shown in Figure 4-4.

The output of the up converter is a low level on channel signal. This signal is sent to the output amplifier.

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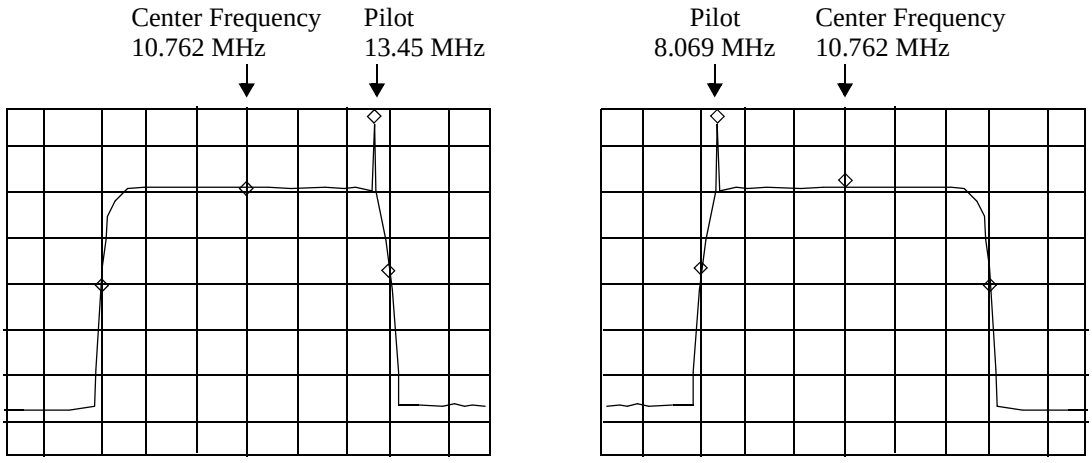

1st IF, Pilot on High side, Channels 2 - 13

1st IF, Pilot on low side, Channels 14 - 69

Figure 4-4 10.762 MHz IF Spectrum

4.4.1.1 Up Converter Board UHF/VHF Band Pass Filter

The type of filter used depends on the operating channel.

In UHF units, an inter digital comb-line band pass filter is used to filter out the mixer image and other unwanted signals. This filter has two tunable sections. A voltage tunable bandpass filter to pass the on channel signal, this is referred to a “TuneB” in the Up Converter Diagnostics screen. It also has a voltage tunable notch filter to reject the local oscillator, this is referred to as “TuneA” in the Up Converter Diagnostics screen. When a UHF channel is selected, the filter is automatically tuned to the correct frequency for that channel. The TuneA and TuneB options in the Up Converter Diagnostics screen allow the two filters to be retuned for testing purposes.

Low band VHF channels 2 - 6 have the local oscillator, 2nd IF frequency and image above the channel, therefore, an elliptic low pass filter with a cutoff frequency of 100 MHz is used for the low band filter. This filter that is capable of passing channels 2 through 6 with low group delay while still rejecting the required signals.

High band VHF channels 7-13 have the local oscillator and image above the channel and the 2nd IF frequency below the channel. For this group of channels, a bandpass filter is required. This is a fixed bandpass filter that is capable of passing channels 7 through 13 with low group delay while still rejecting the required signals.

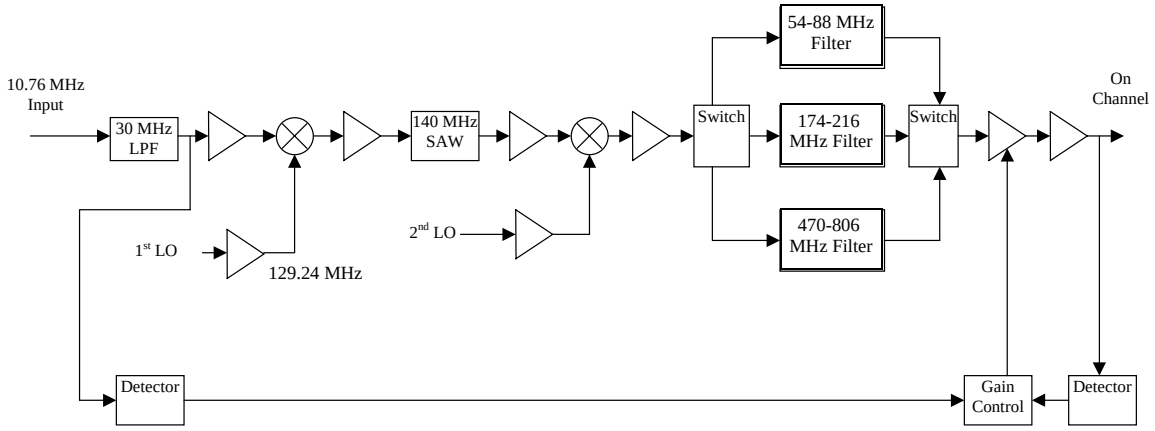

Figure 4-5 Up Converter Simplified Block Diagram.

4.4.2 Down Converter Board Block Diagram Description

Refer to Figure 4-6 for a detailed block diagram of the analog chassis of the APEX exciter, and for a block diagram of the down converter.

The down converter has four inputs, which are RF output samples of the exciter, transmitter IPA, transmitter PA, and HPF (high power filter). These inputs are sequentially sampled, but the exciter RF output is only sampled when the Setup > Display > Chart Source is set to monitor the exciter. The feedback samples are heterodyned down to the 10.762 MHz 1st IF frequency. The conversion process takes place in two steps using the same to local oscillator signals (from the PLL board) as the up converter.

For the RTAC (real time adaptive correction) circuits in the adaptive correction board to work, two RF feedback samples from various points along the transmitter system are required. These samples come from the PA output and the HPF (high power filter) output. The RF level for each sample should be within a range of -10 to 0 dBm average power where the RF sample cables enter the rear panel connectors of the exciter.

The controller board causes the down converter to switch through the IPA, PA and HPF samples. The IPA and PA samples take up to 5 seconds each and the HPF takes 5 to 90 seconds depending on the length and type of waveguide entered in the exciter setup page. These samples normally cycle through in two to four second steps. The sequence is IPA, HPF, Amp, and HPF. The exciter is only sampled when the Setup > Display > Chart Source is set to monitor the exciter.

When a sample is first switched into the down converter, an APC (automatic power control) circuit adjusts the signal to the required level. The RF sample being converted and its RF level (at the output of the down converter) can be viewed in real time on the IF &RF processing Status 4/4 Down Converter Diagnostics screen. The level adjusted output of the down converter is sent to the input of the ADC (analog to digital converter) board in the digital assembly. During the remainder of the sample time, RTAC acts on the sample to produce the appropriate precorrection.

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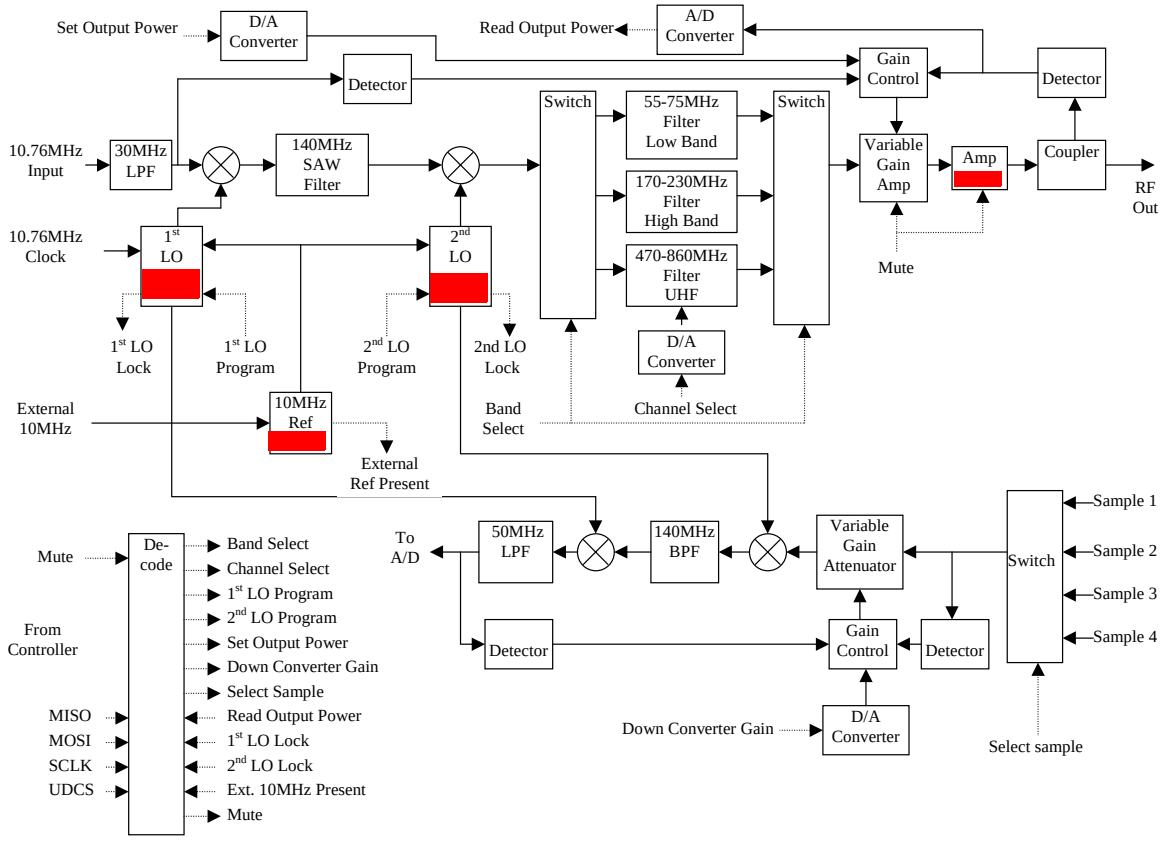

Figure 4-6 Analog Assembly Detailed Block Diagram.

4.4.3 PLL Board - A9

The PLL (phase lock loop) board generates the two local oscillator signals needed for the double conversion used by the up and down converter boards. A 10 MHz reference oscillator is required to keep the two local oscillators on frequency.

4.4.3.1 10 MHz Reference

Refer to Figure 4-7. The primary 10 Mhz reference is generated by OCXO U57. It is buffered by U12 and U19 and two outputs are available. One (J11) is for the first and second local oscillators, one (J8) is unused. This OCXO runs in either of two modes,

The 10 MHz oscillator frequency can be controlled by either of two methods.

- One method is via a control voltage form the tune DAC U40. The DAC number is supplied from PLL Diagnostic screen Xtal Aging (crystal oscillator aging) control. It is used to set the frequency of the internal 10 MHz crystal oscillator when no external 10 MHz reference input is present. Refer to Figure 3-15, PLL Diagnostics, on page 3-17.

- The other method, where precise pilot frequency is required, is to lock the 10 MHz crystal oscillator to an external 10 MHz reference, for example, from GPS.

  If an external 10 MHz reference, with a level within the -10 to +10 dBm range, is supplied, electronic switch U40 automatically switches the OCXO control input from the tune DAC (U40) to the PLL (U29) control voltage output.

In frequency lock mode the OCXO is locked to an external reference via a PLL (ADF4110). Lock time of this PLL is controlled so that the actual reference frequency is ramped between free run and phase lock. This ramp speed minimizes the chance of receiver breakup during application or loss of the external reference. The reference frequency of the PLL is 1kHz. Both R and N counters of the ADF4110 are programmed to divide the signal down to 1000 Hz.

An external 10 MHz input may be applied. If present, the external reference is set to 1V p-p by an AGC circuit. This allows a -10 to +10 dBm range of input level. If sufficient level is present, as determined by a temperature compensated detector, a comparator is set. The external reference and the OCXO are divided down to 10kHz and phase compared. The phase error is used to lock the OXCO to the external source. The loop filter and time constants are such that the frequency difference of the external and internal OXCO is driven to zero. In this way the OXCO and not the external source determine the overall phase noise. This allows use of lower cost GPS based references. A lock detect circuit is also included. It indicates that either external reference is off frequency or the OXCO is beyond its aging limit. Both external 10 MHz present detector and Lock status are available on the front panel.

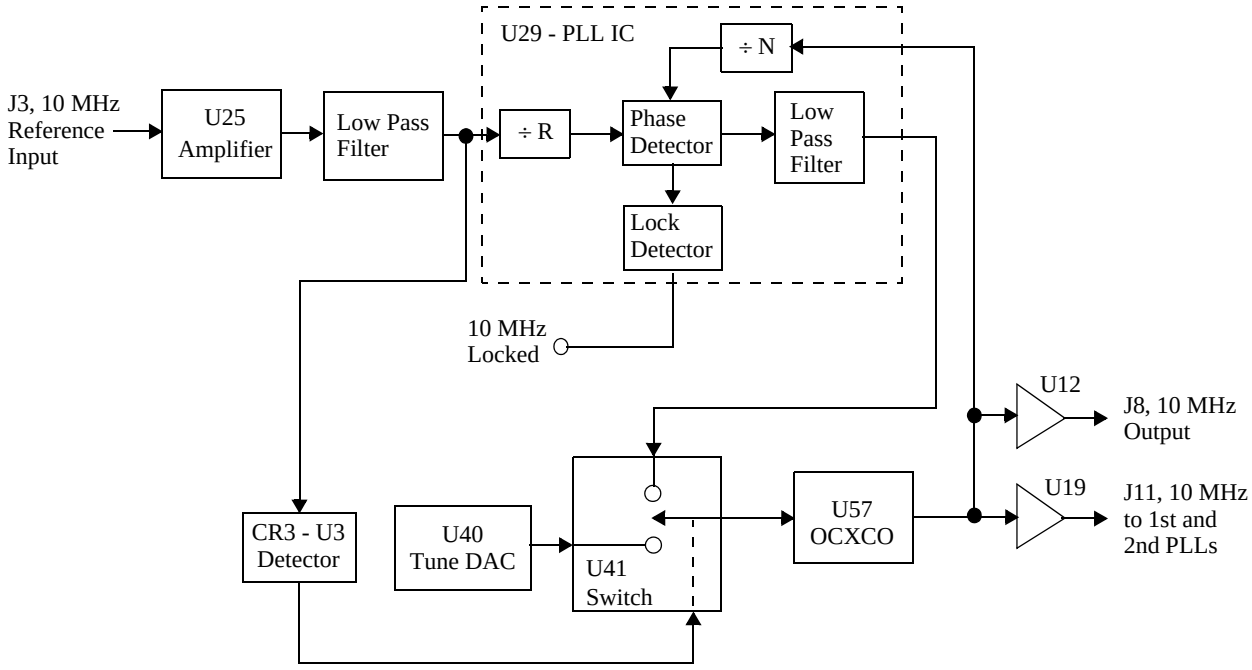

Figure 4-7 10 MHz Reference Oscillator Block Diagram

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4.4.3.2 129.24 MHz IF PLL (First L. O.)

4.4.3.2.1 Introduction

The first local oscillator PLL generates a 129.237762 MHz CW signal. It is used to convert the digitally generated 10.76 MHz 1st IF to the 140 MHz 2nd IF frequency.

4.4.3.2.2 DTV Frequency Problem

A problem exists for all DTV (8VSB) exciters. The tolerance allowed the 19.3926588 MHz transport stream clock is +/-54 Hz. Since the digital tray clocks are locked to the transport stream clock, the 10.762238 and the 43.048952 MHz clocks have a 30 and 120 Hz tolerance respectively. This causes the 10.762238 MHz center frequency 1st IF signal, from the digital to analog converter of the digital tray, to have a proportional frequency tolerances. See Figure 4-4, 10.762 MHz IF Spectrum, on page 4-9.

- The 1st IF pilot, for the VHF channels, is located on the high side of the spectrum, and has a frequency of 13.4527975 MHz with a tolerance of +/-37.5 Hz.
- The 1st IF pilot for the UHF channels is located on the low side of the spectrum, and has a frequency of 8.0716785 MHz with a tolerance of +/-22.5 Hz.

The FCC rules place a restriction of +/-3 Hz on the pilot frequency when a lower adjacent channel analog transmitter is within 88 km of the digital transmitter. This means that the above mentioned pilot frequency tolerance, which results form the transport stream clock frequency variation, must be removed so that the pilot frequency can be controlled down to the Hz. This is accomplished by causing the 1st LO signal to have the opposite transport stream induced frequency tolerance as the pilot. In this way, the pilot frequency variation is tracked out in the first mixer of the up converter.

4.4.3.2.3 PLL Board 1st LO Block Diagram Description

Refer to Figure 4-8, block diagram of the first local oscillator. A 400 MHz oscillator (U42) is phase locked to the 10 MHz reference input. The 400 MHz CW signal clocks a 32 bit DDS (direct digital synthesis) based oscillator (U39), the output of which is:

- 142.6905595 MHz CW signal for VHF channels 2 through 13.
- 137.3094405 MHz CW signal for UHF channels 14 through 69.

Next, the 10.762238 MHz clock, from the digital tray, with its 30 Hz tolerance, is divided by 4 then the following harmonics of the divided clock are selected for VHF and UHF operation.

- For VHF, the 5th harmonic is selected and passed through a bandpass filter, resulting in a frequency of 13.4527975 MHz with a tolerance of +/-37.5 Hz.
- For UHF, the 3rd harmonic is selected and passed through a bandpass filter, resulting in a frequency of 8.0716785 MHz with a tolerance of +/-22.5 Hz.

Notice that these are the same frequencies and tolerances as their respective 1st IF pilots, which are given above.

Finally, the DDS output and the output of the selected, multiplied clock bandpass filter are sent to mixer U28, and the difference selected by filters FL8, FL2, and FL3. This results in the frequency tolerance of the 1st LO output to be the equal to but opposite of its respective pilot frequency tolerance, and therefore, the two tolerances cancel.

As a result, the on channel pilot tolerance is proportional to the 10 MHz reference, which is usually a fraction of a hertz when an external reference is used.

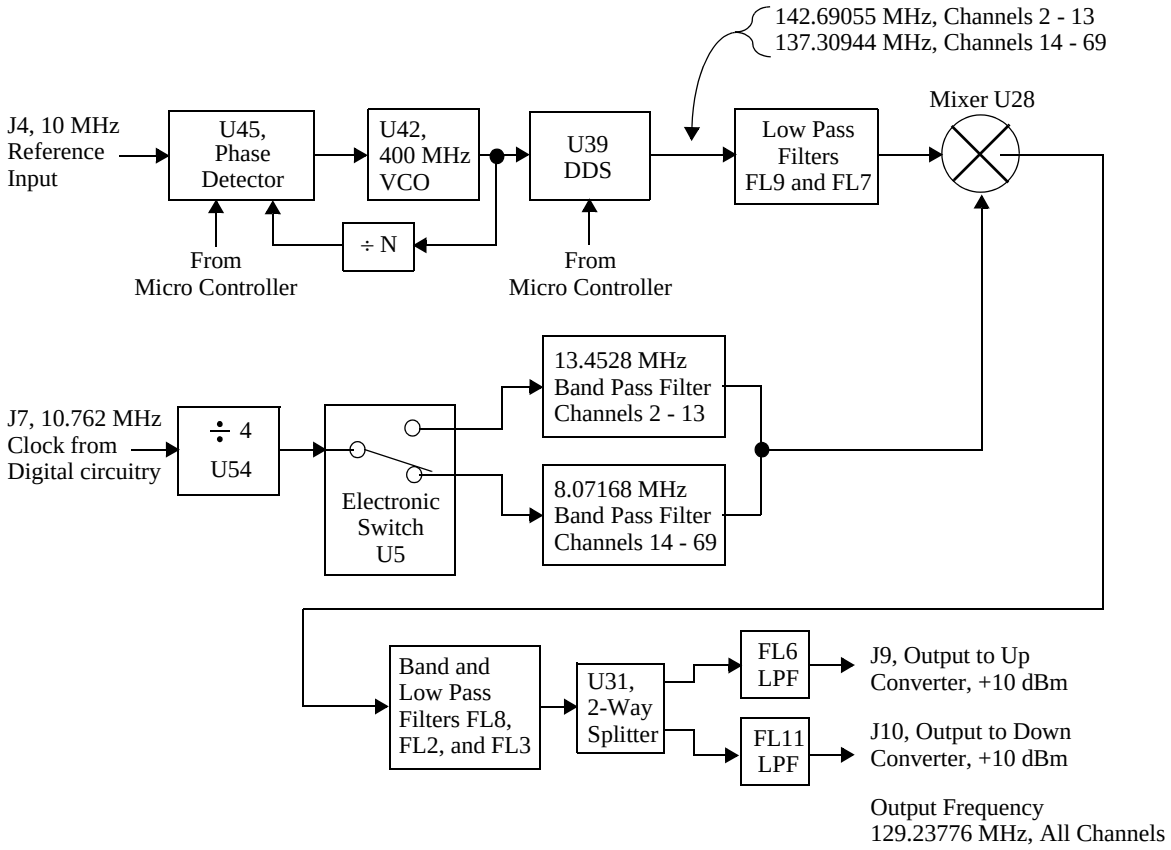
142.69055 MHz, Channels 2 - 13
137.30944 MHz, Channels 14 - 69
Mixer U28
J4, 10 MHz Reference Input
U45, Phase Detector
U42, 400 MHz VCO
U39 DDS
Low Pass Filters FL9 and FL7
÷ N
From Micro Controller
From Micro Controller
J7, 10.762 MHz Clock from Digital circuitry
÷ 4 U54
Electronic Switch U5
13.4528 MHz Band Pass Filter Channels 2 - 13
8.07168 MHz Band Pass Filter Channels 14 - 69
Band and Low Pass Filters FL8, FL2, and FL3
U31, 2-Way Splitter
FL6 LPF
FL11 LPF
J9, Output to Up Converter, +10 dBm
J10, Output to Down Converter, +10 dBm
Output Frequency
129.23776 MHz, All Channels

Figure 4-8 Block Diagram First LO

WARNING: Disconnect primary power prior to servicing.

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4.4.3.3 Main Phase Lock Loop (Second LO)

Refer to Figure 4-9, Second LO Block Diagram.

The second LO covers 197-663 MHz. It is referenced to the 10 MHz reference oscillator, which is locked to GPS. It is used to convert the 140 MHz (center channel) second IF to the desired channel center frequency.

The second local oscillator PLL generates a CW signal which is 140 MHz above the desired center channel frequency for VHF channels and 140 MHZ below the desired center channel frequency for UHF channels. Refer to Table 4-1 for a list of frequencies for channels used within the USA.

A single loop PLL, locked to the 10 MHZ reference oscillator is used to set the 865 MHz to 1180 MHz VCO to a specific frequency within its frequency range. This chosen frequency is applied to a divide by N circuit, where N is chosen so that its output, or a harmonic of its output, falls on the desired second LO frequency. A tunable bandpass filter is controlled via the micro controller to select the desired frequency and assure that the LO output is clean.

Table 4-1 2nd LO Output Frequencies

Channel	Frequency Range	2nd LO Frequency
Standard channels for USA		
2	54 - 60 MHz	197 MHz
4 MHz gap between channels 4 and 5.		
6	82 - 88 MHz	225 MHz
7	174 - 180 MHz	317 MHz
13	210 - 216 MHz	353 MHz
14	470 - 476 MHz	333 MHz
69	800 - 806 MHz	663 MHz

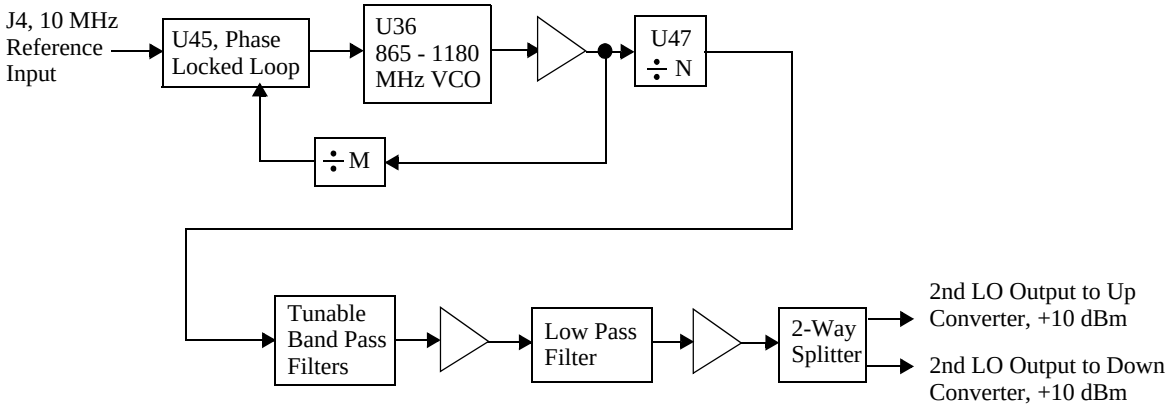
J4, 10 MHz Reference Input
U45, Phase Locked Loop
U36 865 - 1180 MHz VCO
U47 ÷ N
÷ M
Tunable Band Pass Filters
Low Pass Filter
2-Way Splitter
2nd LO Output to Up Converter, +10 dBm
2nd LO Output to Down Converter, +10 dBm

Figure 4-9 Block Diagram Main Phase Lock Loop (2nd LO)

WARNING: Disconnect primary power prior to servicing.

4.4.4 Output Amplifier

The output amplifier accepts an on channel input from the up converter and amplifies the signal up to 250 mW average power. It is broad band and covers the VHF and UHF bands.

The output of the up converter is a low level signal of approximately -11 dBm. The output amplifier provides approximately 35 dB gain to raise the signal level to +24 dBm, which is 250 mW average power (1 watt peak power). The RF output signal intermod performance is as follows:

- -49 dB at 250 mW average output level.
- -52 dB at 125 mW average output level.

RF input is routed from J1 through broad band amplifiers U2 and U4 and to splitter U3. The two outputs of splitter U3 drive two broadband amplifiers U6 and U1 in parallel. The outputs from these two amplifiers are combined in U5. From U5 the RF is routed through directional coupler DC1 then to relay K1, which routes the output to the RF output jack (J2) when the exciter is unmuted, and to the RF load output jack (J3) when muted.

Directional coupler DC1 samples the forward power of the amplifier and routes the sample to splitter U7. One output of U7 drives the detector, which consists of CR3, CR6, U8, U9, and U10. The detection diode CR3 is temperature compensated by CR6 in summing amplifier U9. The dc output of U9 is routed to controller board via the UDC interface board. It is used for APC (automatic power control) of the exciter RF output. The other output of U7 is routed through a 7 dB attenuator (R26, R27, and R29) and provides a 2 dBm RF sample for the exciter input of the down converter board.

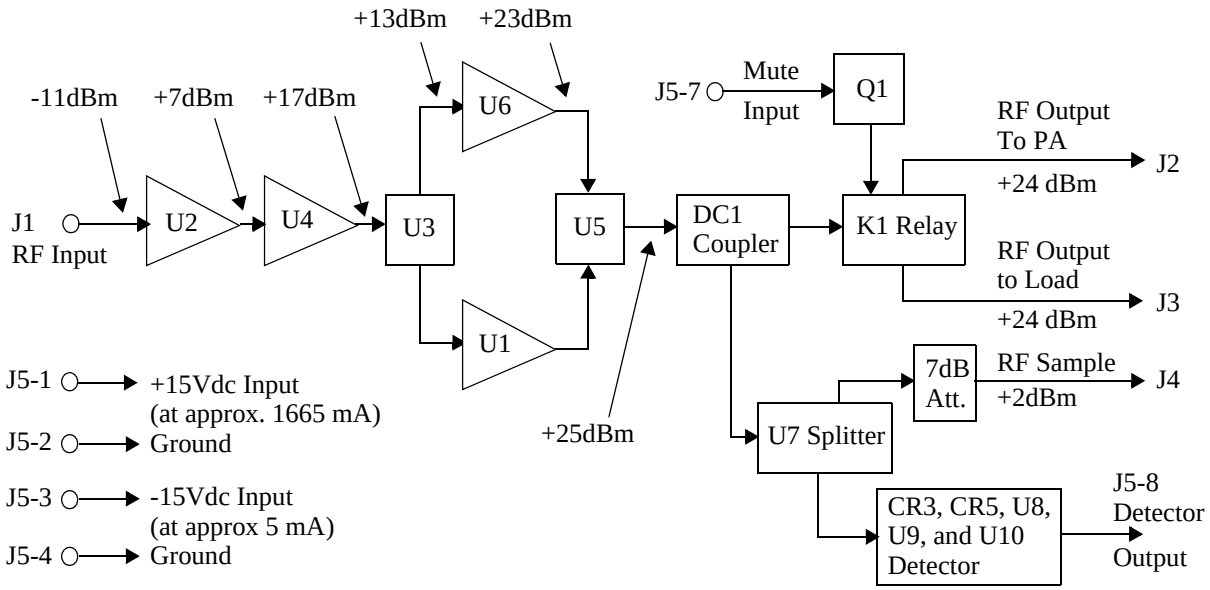

Figure 4-10 Output RF Amplifier Block Diagram

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4.5 DC Power Distribution

This material is intended to give an overview of dc power distribution in the APEX exciter.

4.5.1 Main Power Supply

The main power supply is located in the left rear side of the analog (top) section of the exciter. The main power supply voltages and their destinations are listed in Table 4-2.

Table 4-2 Exciter Power Supply Voltages

Voltage	Use	PS Jack and Pin	Destination Jack and Pin
+5 Vdc	Power for digital tray	SK3 pin 2	Controller, J6 pins 10 - 13
Common for +5 V		SK3 pin 1	Controller, J6 pins 1 - 4
+15	Power for analog tray	SK2 pins 1 - 2	UDC Interface, J4 pins 1 - 2
-15	Power for analog tray	SK2 pin 6	UDC Interface, J4 pin 6
Common for +/- 15 Vdc		SK2 pins 3 - 5	UDC Interface, J4 pins 3 - 5
+15 Vdc Float	Fan power	SK2 pin 8	UDC Interface, J4 pin 8
Common for +15 Vdc Float		SK2 pin 9	UDC Interface, J4 pin 9

4.5.2 Digital Deck Power

All power for the digital (lower) deck of the exciter enters the controller board at J6.

Refer to Figure 5-2, on page 5-3. From the controller board the power branches out to the other digital boards in the following fashion.

- Controller board to modulator board to SMPTE 310 board.
- Controller board to adaptive corrector board to ADC and DAC boards.
- Controller board to external I/O board.
- Controller board to front panel board.

4.5.2.1 Controller Board Power

All power for the digital (lower) deck of the exciter enters the controller board at J6. J6 is mounted on the chassis side of the board and protrudes through the deck to the top side, where it receives +5 Vdc from the power supply on pins 9 through 15. The 5Vdc return (ground) is via pins 1 through 8. This is the 5 Vdc entry on the screen.

+5 Vdc is supplied to the following other boards:

- The modulator board.
- The adaptive precorrector board.
- The external I/O board.
- The front panel display board.

The +5 Vdc also operates the 3.3 volt dc to dc converter. +3.3 Vdc from this board is supplied to the following boards:

- The external I/O board.
- The front panel display board.

WARNING: Disconnect primary power prior to servicing.

The following are the controller board status screen entries:

- +3.3 Vdc: This is the output of the 3.3 V dc to dc converter.
- +5 Vdc: This is the board input voltage.

RTC battery: (OK or FAULT) This is the battery required for the real time clock.

4.5.2.2 Modulator Board Power

The modulator board receives +5 VDC from the controller board. This is the 5 Vdc entry on the screen.

+5 Vdc is supplied to the SMPTE 310 Interface board.

The +5 Vdc also operates two dc to dc converters which supply the 3.3 Vdc and 1.8 Vdc.

+3.3 Vdc from the dc to dc converter is supplied to the SMPTE 310 Interface board.

The following are the modulator board status screen entries:

- +3.3 Vdc: This is the output of the 3.3 V dc to dc converter.
- +5 Vdc: This is the board input voltage.
- DSP 3.3 Vdc supply (referred to as the MOD_IOVDD supply) is derived from the 3.3 Vdc supply through an FET switch. This voltage is switched off if the DSP 1.8 Vdc supply faults.
- DSP 1.8 Vdc (called MOD_CVDD) core power supply.
- 3.3 V PS: (OK or FAULT) refers to the output of the 3.3 volt dc to dc converter.
- 1.8 V PS: (OK or FAULT) refers to the output of the DSP 1.8 volt supply.

4.5.2.3 SMPTE 310 Board Power

SMPTE 310 board receives +5 VDC and +3.3 VDC from the modulator board. These two voltages appear on the SMPTE 310 board status screen:

4.5.2.4 Adaptive Processing Board Power

The adaptive precorrector board receives +5 VDC from the controller board. This is the 5 Vdc entry on the screen.

The +5 Vdc also operates three dc to dc converters which supply the +3.3 Vdc, +1.9 Vdc, and the +1.8 Vdc voltages.

+5 Vdc and +3.3 Vdc are supplied to the D/A converter and the A/D converter.

The following are the adaptive processing board screen entries:

- +3.3 Vdc: This is the output of the 3.3 V dc to dc converter.
- +5 Vdc: This is the board input voltage.
- AP 3.3 Vdc supply (referred to as the AP_IOVDD supply) is derived from the 3.3 Vdc supply through an FET switch. This voltage is switched off if the 1.9 Vdc AP supply faults.
- AP 1.9 Vdc: This is the output from the AP DSP core supply dc to dc converter

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- NL 3.3 Vdc supply (referred to as the NL_IOVDD supply) is derived from the 3.3 Vdc supply through an FET switch. This voltage is switched off if the 1.8 Vdc NL supply faults.
- NL 1.8 Vdc NL DSP core power supply.

4.5.2.5 Power for DAC and ADC Boards

5 Vdc and +3.3 Vdc are supplied to the DAC (digital to analog converter) and ADC (analog to digital converter) from the adaptive corrector board.

4.5.2.6 External I/O Board Power

5 Vdc and +3.3 Vdc are supplied to the external I/O board is received at connector P1 from controller board connector J3.

4.5.2.7 Front Panel Board

Power for front panel board is received at connector J1 from controller board connector J4.

- +5 Vdc for the front panel board is received at connector J1 pins 1 and 2.
- +5 Vdc for the back light is received at connector J1 pins 46 through 50.
- +3.3 Vdc for the front panel board is received at connector J1 pins 24 and 25.

4.5.3 Analog Deck Power

All power for the analog (upper) deck of the exciter enters the UDC interface board at J4.

From the UDC interface board J2 the power is fed to the down converter board J8, PLL board J1, and up converter board J3 by a ribbon cable which parallels the connectors.

4.5.3.1 UDC Interface Board Power

The power supply module supplies +/- 15 Vdc to the UDC (up/down converter) Interface board via connector J4. See Table 4-2 on page 17 for a list of pin assignments for J4.

+15 Vdc is fed to an on-board switching dc to dc converter and produces +8 Vdc. +8 Vdc is fed to a linear regulator which produces +5 Vdc. +5 Vdc is fed to a linear regulator which produces +3.3 Vdc.

The +/-15 Vdc and the +8 Vdc voltages are fed from the UDC interface board J2 to the down converter board J8, PLL board J1, and up converter board J3 by a ribbon cable which parallels the connectors. The output amplifier receives +/-15 Vdc at J5 from the up converter board via J2. The ribbon cable pinout is as follows:

- +15 Vdc pin 1.
- -15 Vdc pin 3.
- +8 Vdc pin 5.
- Ground (returns) are pins 2 and 4.

The following ia a list of entries on the UDC interface board status screen.

- +15 Vdc: Input from power supply module

- -15 Vdc: Input from power supply module
- 5 Vdc: Output from 5 volt linear regulator.
- 3.3 Vdc: Output from 3.3 volt linear regulator.
- 8 Vdc: Output from 8 volt switching regulator

4.5.3.2 Exciter Cooling Fan Power

Power for the exciter cooling fan is routed through the UDC interface board as follows

- +15 Volt Float is received at UDC interface board at J4 pin 8, the return is J4 pin 9.
- +15 Volt Float leaves UDC interface board at J5 pin 2, the return is J5 pin 1.

4.5.3.3 Down Converter Board Power

The down converter board receives its dc voltages (+/- 15 Vdc and +8 Vdc) from the UDC interface board via connector J8. The down converter board supplies are listed below.

- +15 Vdc: Input power from UDC interface board via connector J8 pin 1
- -15 Vdc: Input power from UDC interface board via connector J8 pin 3
- 8 Vdc: Input power from UDC interface board via connector J8 pin 5
- An on board regulator produces -5 Vdc from the -15 Vdc supply
- An on board regulator produces +5 Vdc from the +8 Vdc supply.

The following ia a list of entries on the down converter board status screen.

- +15 Vdc: Input power
- -15 Vdc: Input power
- +8 Vdc: Input power.

4.5.3.4 PLL Board Power

The PLL (phase lock loop) board receives its dc voltages (+/- 15 Vdc and +8 Vdc) from the UDC interface board via connector J1, as listed below.

- +15 Vdc: Input power from UDC interface board via connector J1 pin 1
- -15 Vdc: Input power from UDC interface board via connector J1 pin 3
- 8 Vdc: Input power from UDC interface board via connector J1 pin 5

In order to achieve low noise and excellent isolation between the PLL board digital input/output circuits, 10 MHz reference oscillator, 129.24 MHz 1st local oscillator (LO), and the 2ns local oscillator, this board contains eight on board +5 Vdc regulators and one +12 Vdc regulator. The regulators are

- +5V_Buf and +5V_Stat for the digital circuits.
- +5V_Div and +5V_Pll2 for the 2nd local oscillator circuits.
- +5V_DDS, +5V_Pilot, and +5V_Pll for the 1st local oscillator circuits.
- +12VReg and +5V_10M for the reference oscillator circuits.

The following ia a list of entries on the PLL board status screen.

- +15 Vdc: Input power from UDC interface board via connector J1 pin 1.

- -15 Vdc: Input power from UDC interface board via connector J1pin 3.
- 8 Vdc: Input power from UDC interface board via connector J1pin 5.

4.5.3.5 Up Converter Board Power

The Up Converter board receives its dc voltages (+/- 15 Vdc and +8 Vdc) from the UDC interface board via connector J3. The up converter board supplies are listed below.

- +15 Vdc: Input power from UDC interface board via connector J1 pin 1
- -15 Vdc: Input power from UDC interface board via connector J1 pin 3
- 8 Vdc: Input power from UDC interface board via connector J1 pin 5
- An on board regulator produces +5 Vdc from the +15 Vdc supply.

+/-15 Vdc is supplied to the output amplifier from the Up Converter board via J2.

- +15 Vdc is supplied via J2 pin 1.
- -15 Vdc is supplied via J2 pin 3.
- Returns (ground) for the +/-15 volt supplied is via J2 pins 2 and 4.

The +15, -15, and +8 Vdc inputs appear on the up converter board status screen.

4.5.3.6 Output Amplifier

Power for the output amplifier is received at J5 from the up converter board via J2. The power connections for J5 are listed below.

- +15 Vdc is received at J5 pin 1.
- -15 Vdc is received at J5 pin 3.

Returns (ground) for the +/-15 volt supplies are via J5 pins 2 and 4.

5 Maintenance and Troubleshooting

This section is a maintenance and troubleshooting guide to the APEX exciter. Trouble shooting is to the board level only, if a board is defective it should be replaced.

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5.1 Exciter Maintenance

All APEX circuit boards except the front panel board can be accessed while operating the exciter. The APEX exciter is mounted in the transmitter on slides, permitting it to be pulled forward out of the cabinet.

The top and bottom covers can be removed to provide access to the digital and analog circuit boards. Figure 5-1 shows the top (analog) view and Figure 5-2 shows the bottom (digital) view of the exciter with the covers removed. These drawings provide the names and locations of the various circuit boards of the exciter.

The upper side of the chassis is the analog section, which consists of the up converter, down converter, PLL (phase lock loop), RF output amplifier, power supply, UDC (up/down converter) interface board, and the exciter cooling fan.

The bottom side of chassis houses the SMPTE 310M interface, modulator, adaptive pre corrector, DAC (digital to analog converter) converter, ADC (analog to digital converter), controller, and the external I/O (input/output) interface boards.

If the exciter is being bench tested and is inverted to access the bottom boards, the display can also be inverted by accessing Display Invert function. The path to this function is Main screen > Setup > Display.

The exciter wiring diagram is shown in Figure 5-3 (left side of drawing) and Figures 5-4 or 5-5 (right side of drawing). Figure 5-4 shows the 901-0121-061 PLL board and Figure 5-5 shows the 992-0121-061 PLL board. The left side and right side pages of this drawing can be printed and fastened together to produce one complete drawing.

5.1.1 Cleaning

Occasionally the circuit boards of the exciter will need cleaning. All precaution against static should be observed. The technician should be grounded, either through conductive shoes or through a static grounding strap.

The exciter should be powered down before the cleaning process is started. A vacuum cleaner should be used to remove dust from the assemblies. A natural bristle brush with a metal band and a wooden handle can be used to dislodge dust. A vacuum cleaner hose can develop static due to the air rushing through the hose. The hose should have a metal nozzle, which should be grounded.

Do not use compressed air to blow dirt from the exciter because the dirt will just settle back down on something else. Also, the fast moving air could damage or dislodge delicate circuit board components, and it could also accentuate static problems.

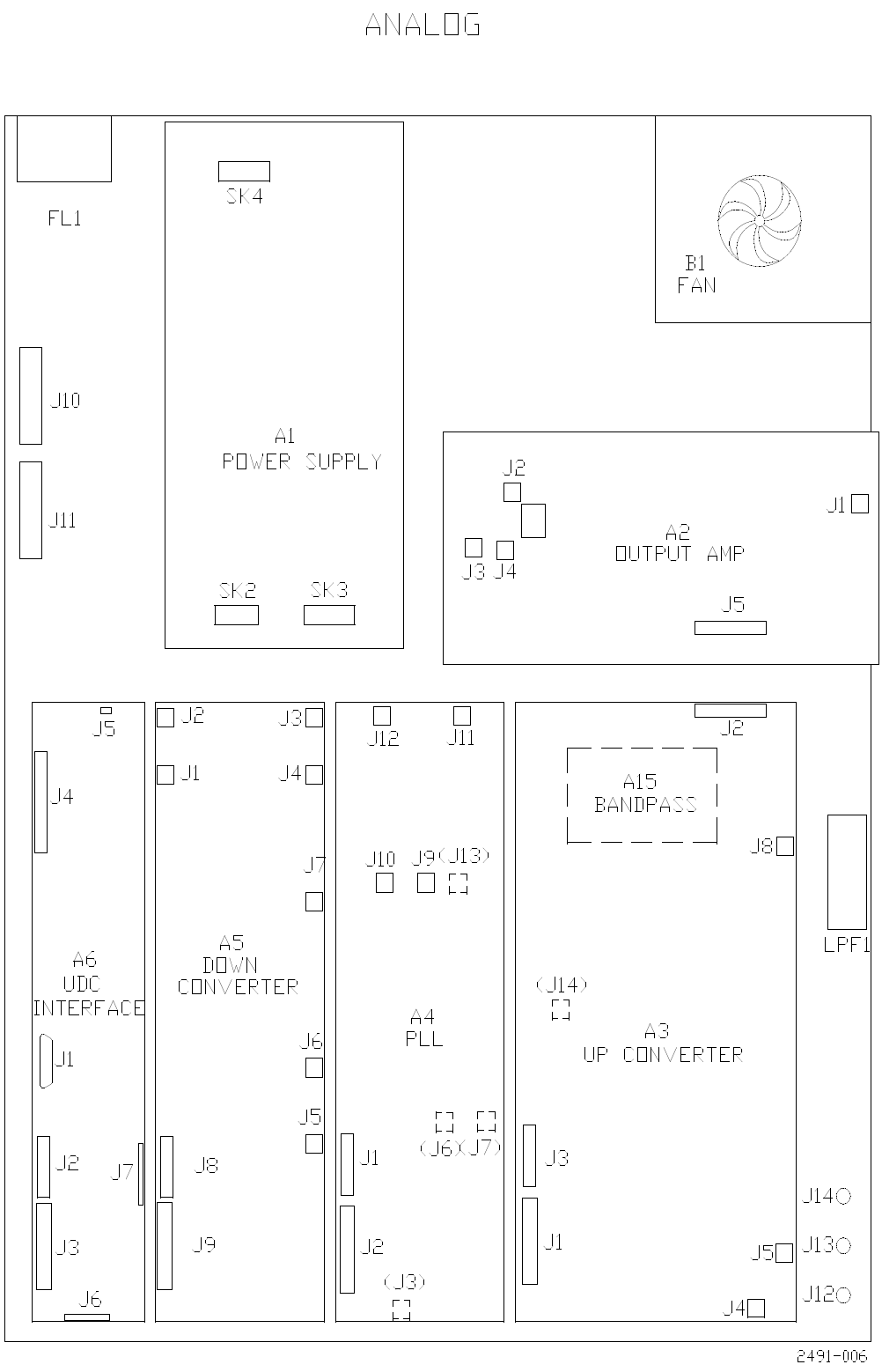

Figure 5-1 Top View of Exciter (Analog Side) With Cover Removed

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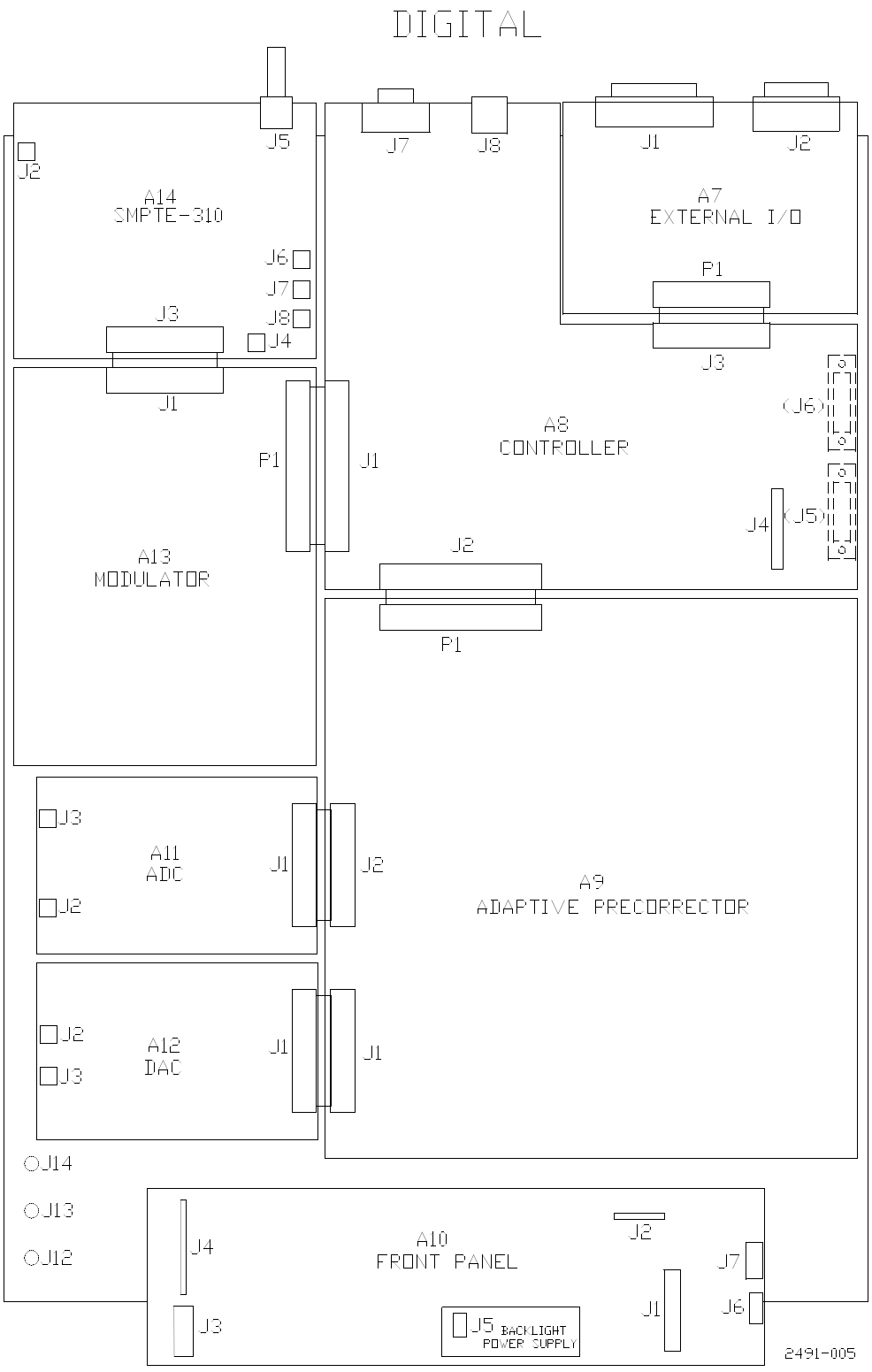

Figure 5-2 Bottom View of Exciter (Digital Side) With Cover Removed

WARNING: Disconnect primary power prior to servicing.

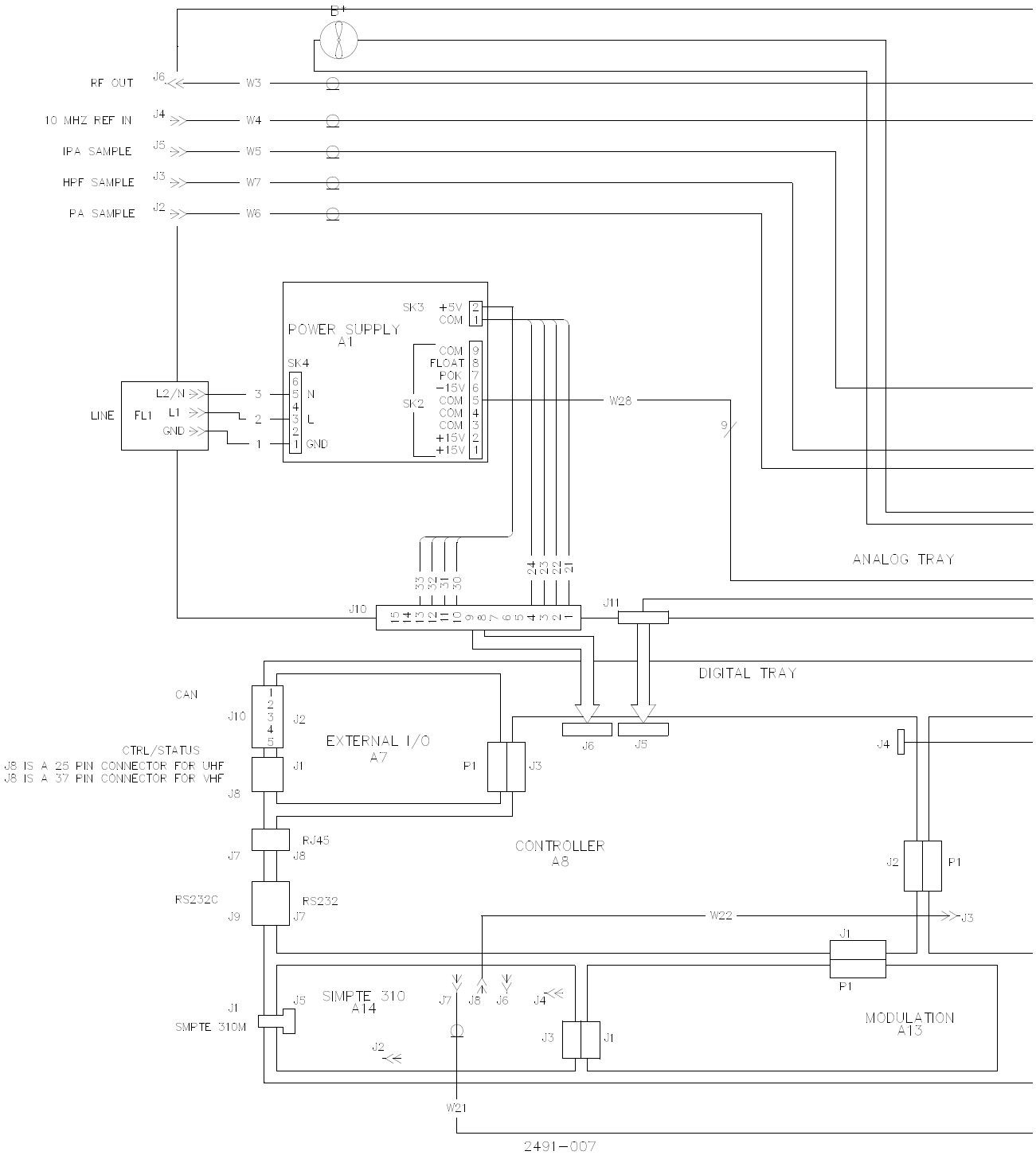

Figure 5-3 APEX Exciter Wiring Diagram, Left Side (see Figure 5-4 for right side)

WARNING: Disconnect primary power prior to servicing.

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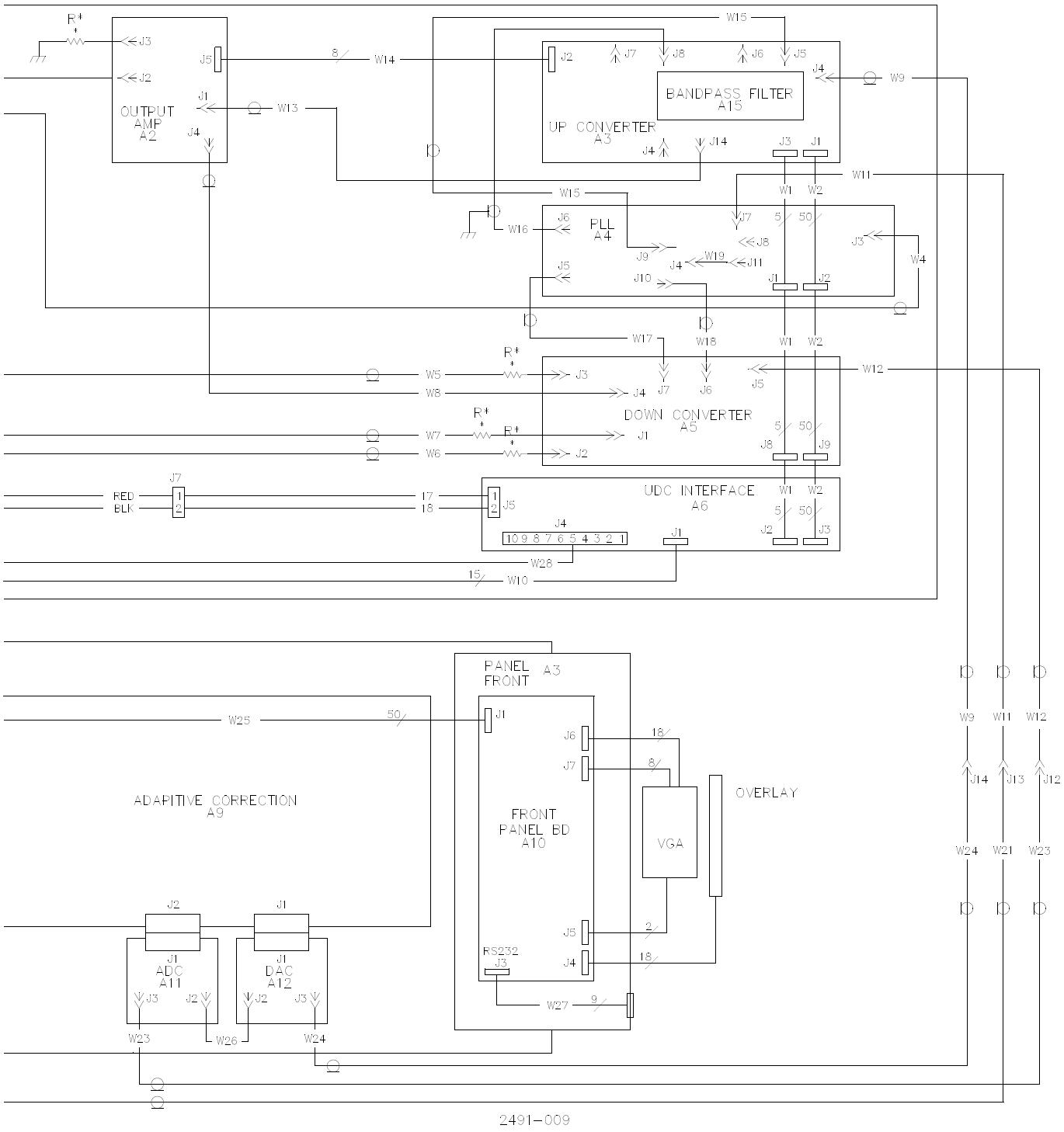

Figure 5-4 APEX Exciter Wiring Diagram, Right Side, 901-0121-061 PLL Board (see Figure 5-3 for left side)

WARNING: Disconnect primary power prior to servicing.

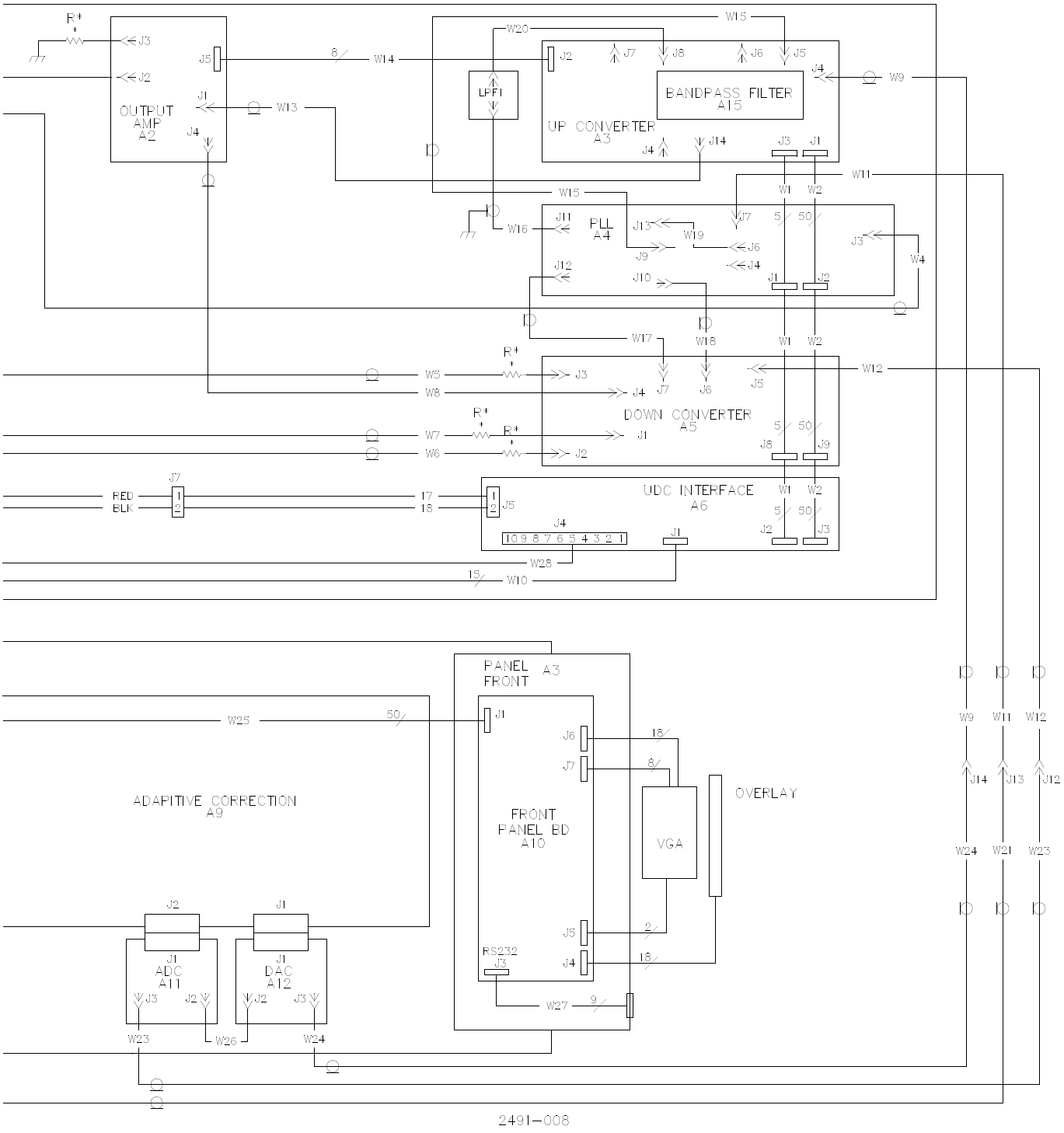

Figure 5-5 APEX Exciter Wiring Diagram, Right Side, 992-9995-017 PLL Board (see Figure 5-3 for left side)

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5.1.2 SMPTE 310 Board 43 MHz oscillator Frequency

The exciter 43.048 MHz clock, 10.762 MHz clock, and the 10.76 MHz symbol rate are controlled by a 43.048MHz oscillator. This oscillator is phase-locked to the incoming 19.39Mbit data clock.

Over time, it is expected this oscillator will age and will require occasional adjustment. The oscillator aging adjustment is performed on the touch screen. The path to this adjustment is Main Screen > Status > MPEG Input Status > Diagnostics >MPEG Input Diagnostics screen.

Refer to Figure 3-7, on page 3-10. EEPot value is changed to compensate for aging of 43 MHz crystal. Values range from 0 to 1023 with the default value being 0. The new number is entered via touch screen key pad. If this setting is changed, the new value will remain after an AC power loss.

Changing this setting causes the 43MHz oscillator control voltage to change. The control voltage is obtained from the output of the PLL, which locks the 43 MHz oscillator to the 19.39 MHz transport stream clock. The control voltage can be viewed on the MPEG Input Status screen. Typical range for the control voltage is 2.23 to 2.34 volts, with 2.28 volts being nominal.

Procedure for setting SMPTE board 43 MHz oscillator.

1 Select one of the test patterns (except Loopback) in the SMPTE Test Pattern selection of the Exciter Setup screen.

2 Measure 19.39 MHz oscillator at J2 on SMPTE board. The frequency should be 19.392659 MHz +/- 54 Hz. If this oscillator is out of tolerance, it will effect the 43.048 MHz oscillator.

   A The 19.39 MHz oscillator has a mechanical adjustment (on the oscillator case) which can be used to set the frequency if it is out of tolerance.

3 Set the EEPot in the MPEG Input Diagnosis screen, number range is 0 to 1024, so that the 43 MHz Control voltage is 2.28 VDC.

4 This procedure is complete, return the exciter to normal.

5.1.3 Measuring and Setting Pilot and PLL Board Frequencies

When not using an external 10 MHz reference, the internal 10 MHz reference oscillator in the PLL board ultimately determines accuracy of the pilot frequency at the output of the exciter. Therefore, the pilot frequency at the output of the exciter is the measurement reference used when setting the internal 10 MHz oscillator XTAL Aging (crystal oscillator aging) potentiometer.

Pilot frequency accuracy is directly dependant on the accuracy of the 1st and 2nd local oscillators (LOs) in the PLL board, which get their reference from the 10 MHz reference oscillator. If a large pilot frequency error exists, check the PLL status screen (second of four IF & RF processing status screens) for faults. If one or more faults appear on this screen, refer to Section 5.8.1 on page 5-22 for additional troubleshooting information.

Before the subject of setting the 10 MHz reference frequency is attempted, it is necessary to measure the pilot frequency.

5.1.3.1 Measuring the Pilot Frequency

Since the ATSC signal is wide band and noise-like, measurement of the transmitter output frequency during program transmission may not be possible, unless suitable test equipment is available.

A special procedure which removes all transmitted data, leaving only the pilot, allows the pilot frequency to be directly measured at the exciter output. A suitable frequency counter will be needed.

Caution

Do not operate the pilot measurement procedure while exciter is providing drive to an operating transmitter. This will cause the pilot output to rise sharply and may cause overloads or even equipment damage.

Note

Unless the frequency counter is locked to an accurate external reference, such as the 10 MHz output of a GPS receiver, it may have an error of 20 Hz or more. Counters will exhibit greater error at UHF then at VHF.

This measurement should be taken while using the alternate exciter, in a dual-exciter transmitter, or by turning the transmitter OFF.

1 Connect the output of the exciter to a frequency counter, using pads as necessary to prevent damage to the input circuit of the counter.

2 On the Status > Digital Processing > Modulator Board > Modulator Diagnostics screen, switch the Nyquist Filter Data from Enabled to Disabled using the screen soft keys.

   A This leaves only the pilot at the output of the exciter.

3 Measure the pilot frequency.

   A Make sure any frequency offsets are taken into account when measuring the pilot frequency. Offsets can be found in the Exciter Setup screen.

   B With no pilot frequency offset, the pilot frequency can be determined by adding 0.309441 MHz to the lower channel frequency limit (in MHz).

4 When this procedure is complete switch the nyquist data back on by changing the Modulator Diagnostics screen Nyquist Filter Data from Disabled to Enabled.

5 Restore the transmitter connections and resume normal operation.

Pilot frequency error can be caused by several factors, which are listed below.

- Wrong channel selected in the exciter setup screen.
- Error in exciter setup screen frequency offset. This entry sets the pilot frequency offset (if required) from the normal pilot frequency for that channel. Pilot frequency offset calculation is covered in Chapter 6, Offset Frequency Calculation.
- 1st and 2nd local oscillator frequency errors caused by internal 10 MHz reference oscillator errors. The solution for this is to set the reference oscillator frequency, this is covered in the next section of this chapter, or to use an external 10 MHz reference if the required pilot frequency tolerance is within a few hertz.
- 1st or 2nd local oscillator frequency errors caused by a faulty PLL board.

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5.1.3.2 PLL Board 10 MHz Reference Oscillator Frequency

In an **external reference is being used**, and it is within the correct level (-10dBm to +10dBm) there is no provision for the 10 MHz reference oscillator frequency adjustment. The accuracy of the 10 MHz output is dependant on the accuracy of the external 10 MHz reference signal. IF a frequency error still exists, check the Status > IF & RF Processing > IF & RF Processing Status 2/4 PLL Board Screen. The Ext. Reference should indicate yes, if it indicates no, it is not receiving the external reference due to a reference signal level problem or a PLL board fault. If the Ext. Reference indicate yes, the 10 MHZ PLL Lock should also indicate yes. Also, the RF PLL Lock, and the IF PLL Lock should all indicate yes.

If **no external reference is being used**, the Status > IF & RF Processing > IF & RF Processing Status 2/4 PLL Board Screen. The Ext. Reference and the 10 MHZ PLL Lock should both indicate no, and the RF and IF PLL Lock indications should both be yes.

The 10 MHz reference internal oscillator frequency is set with the crystal oscillator aging potentiometer. Adjustment provision for this potentiometer is located on the Status > IF & RF Processing > IF & RF Processing Status 2/4 PLL Board > Diagnostics Screen.

This screen has an Xtal Aging (crystal oscillator aging) control. It is used to set the frequency of the internal 10 MHz crystal oscillator. The process is given below.

1 The PLL board 10 MHz reference output connectors (J8 and J11) are mounted on the bottom of the board and are not easy to access. Therefore, the pilot frequency or the 2nd LO frequency can be used to set the 10 MHz oscillator frequency.

2 If the pilot frequency is to be used, refer to Section 5.1.3.1 on page 5-8 for instructions concerning pilot frequency measurements.

   If the 2nd LO is to be used, continue on to setup A.

   A Connect output of 2nd local oscillator to frequency counter. A convenient place to find this output is at J5 or J6 on the PLL board, the output level is +10 dBm.

   If this exciter must remain on the air during this test, do not use J6, it will take the exciter off the air. Use J5, but first put the main screen RTAC functions on Hold before removing the existing cable from J5. Removing the cable from J5 will interfere with normal RTAC adaptation operation.

   B The 2nd local oscillator frequency can be determined from Table 4-1, 2nd LO Output Frequencies, on page 4-15

3 Adjust the Xtal Aging control to produce the correct the pilot or 2nd local oscillator frequency.

   A Adjust the digital potentiometer setting (0 to 4095) by pressing the up or down soft key arrows or touching the number between the arrows to reveal the number touch pad.

   B Higher numbers increase the 10 MHz oscillator and 2nd LO frequencies, increase the pilot frequency in the UHF band, and decrease the pilot frequency in the VHF band.

4 The procedure is now complete. Restore all connections to normal and normalize all settings by comparing them to Table 5-1, Diagnostics Screens Default Settings, on page 5-12 and Table 5-2, Typical Settings For Some of the More Critical Exciter Setup Functions, on page 5-13.

5.1.3.3 Measuring the 1st Local Oscillator Frequency

If it becomes necessary to measure the 1st LO frequency, follow the procedure below.

If this exciter must remain on the air during this test, put the main screen RTAC inputs on Hold before performing this measurement. Removing the cable from J10 of the PLL board will interfere with normal RTAC adaptation operation.

1 Connect output of 1st local oscillator to frequency counter. This signal can be obtained from J10 on the PLL board. It is also available at J9, but disconnecting the cable from it will take the exciter off the air.

   A The output level should be +10 dBm.

2 The 1st local oscillator frequency is affected by both the 10 MHz reference oscillator and the 10.762 MHz clock. The 10.762 MHz clock is input at J7 (on the bottom side of the PLL board) and is obtained from J7 on the SMPTE 310 board.

   A The 10 MHz reference comes from the PLL board 10 MHz reference oscillator, which may be phase locked to an external 10 MHz reference.

   B The 1st LO frequency will change in the opposite direction as the frequency of the 10.762 Mhz clock. The 10.762 MHz clock frequency can be measured at J6 on the SMPTE 310 board.

   C If both the 10 MHz reference oscillator and the 10.762 MHz clock are on frequency, the 1st LO frequency will be 129.237762 MHz.

   If the reference oscillator is off frequency, the 1st LO frequency will change by an amount equal to 12.9 times the frequency error of the reference oscillator.

   If the 10.762 MHz clock is off frequency, the 1st LO frequency will change by an amount equal to +/-3/4 of the frequency error of the 10.762 MHz clock. The correct 10.762 MHz clock frequency is 10.762238 MHz.

   For example, if the 10 MHz reference oscillator is 4 Hz high and the 10.762 MHz clock is 20 Hz low, the expected 1st LO frequency error would be (4 x 12.9) - (-20 x 0.75) or 65.4 Hz high, for a frequency of 129.237827 MHz

3 When measurement is finished, normalize exciter connections and screen settings.

5.1.3.4 Measuring the 2nd Local Oscillator Frequency

If it becomes necessary to measure the 2nd LO frequency, follow the procedure below.

1 Connect output of 2nd local oscillator to frequency counter. A convenient place to find this output is at J5 or J6 on the PLL board, the output level is +10 dBm.

   A If this exciter must remain on the air during this test, do not use J6, it will take the exciter off the air. Use J5, but first put the main screen RTAC functions on Hold before removing the existing cable from J5. Removing the cable from J5 will interfere with normal RTAC adaptation operation.

   B The 2nd local oscillator frequency can be determined from Table 4-1, 2nd LO Output Frequencies, on page 4-15

2 When the procedure is complete, restore all connections to normal.

3 If the 10 MHz reference oscillator is off frequency, the 2nd LO frequency will change by an amount equal to the 10 MHz reference frequency error times the expected 2nd LO frequency divided by 10.

For example, the 2nd LO frequency should be 549 MHz for channel 50. If the 10 MHz reference frequency measured 10.000020 Mhz, the 2nd LO frequency would be 20 x 54.9 or 1098 Hz high, for a frequency of 549.001098 MHz.

4 When measurement is finished, normalize exciter connections and screen settings.

5.2 Loading Software

The APEX exciter software must be occasionally reloaded to update the software to the latest revision, or if the controller board has been changed and contains an incorrect version.

The controller board contains the software, user setups, and the MAC address, all of which will be lost if the controller board is changed. User setups and the MAC address are programmed in the sub windows of the Home > Setup Screen.

APEX exciter software is loaded through the serial port on the front or rear panel of the exciter (following the instructions provided with the software). The serial port used for the software upgrade must be set up to use the Harris protocol. See Section 3.6.5.1, Serial Setup Screen 1 of 3, RS-232, on page 3-40 for serial port programing instructions.

Four items are needed to load software into the Apex exciter, they are:

- The Harris ISP (In-System Programming) Revision 2.0 software (used to load software into the exciter).
- The exciter upgrade software.
- The APEX software programming instructions (for the version of software to be loaded).
- A computer with an operating system specified in the software loading instructions (at the time of this writing it specified windows NT 4.0, 2000 Professional, or XP).

The Harris ISP 2.0 program, upgrade software and software loading instructions can be downloaded from the Harris Premier website or obtained by contacting Harris Technical support.

Please note that Harris ISP 2.0 must be used. Harris ISP 1.10, which comes loaded on the Diamond and Sigma transmitter GUI, is not compatible with APEX.

Proceed with the loading operation following the APEX software programming instructions mentioned above.

WARNING: Disconnect primary power prior to servicing.

5.3 Default Settings For DIagnostics Screens

The diagnostics functions are useful for testing and troubleshooting the exciter, but if left in the wrong position, the transmitter or exciter will not function properly. Table 5-1 is a quick reference for the default diagnostics settings.

Table 5-1 Diagnostics Screens Default Settings

Status Screen With Diagnostics	**Text Location Within Manual**	**Variable**	**Default Setting**
MPEG Input	Section 3.4.2.1, MPEG Input Diagnostics, on page 3-10	EEPot (43.048 MHz Osc. PLL Adjust)	0, see note 1
Adaptive Processing	See Section 3.4.3.1, Adaptive Processing Diagnostics, on page 3-12	Loopback (choices None, Analog, or Digital)	None
		Test Tones	Disabled
Digital Processing (Screen 1of 2)	Section 3.4.4.1.1, Modulator Diagnostics, on page 3-14	Nyquist Filter Data (disabled causes exciter to output pilot only)	Enabled
		Nyquist Test Pattern	Disabled
RF & IF Processing (Screen 2 of 4)	Section 3.4.5.2.1, PLL Diagnostics, on page 3-17	Crystal Aging (Internal 10 MHz Reference Osc)	3500, see Note 2
RF & IF Processing (Screen 3 of 4)	Section 3.4.5.3.1, Up Converter Diagnostics, on page 3-18	Output Power AGC	Enabled
		Tune A (UHF up converter tunable notch filter)	Values depend on UHF channel, see Note 3
		Tune B (UHF up converter tunable B. P. filter)	
RF & IF Processing (Screen 4 of 4)	Section 3.4.5.4.1, Down Converter Diagnostics, on page 3-20	RF Sample Select (at down converter input)	Automatic
		RF Sample AGC (sets down converter output level)	Enabled
System Control (Screen 1 of 4)	Section 3.4.6.1.1, Controller Board Diagnostics, on page 3-22	Bit Fifo Test Pattern, used by engineering. If enabled, will block normal 8-VSB signal flow.	Disabled
System Control (Screen 2 of 4)	Section 3.4.6.2.1, External I/O Diagnostics, on page 3-24	Analog Loopback	Disabled
		Analog Output A	0
		Analog output B	0
System Control (Screen 3 of 4)	Section 3.4.6.3.1, CAN Diagnostics, on page 3-25	A CAN Test Message is available	Disabled
Note 1. The default EEPot (43.048 MHz Osc. Adjust) value of zero may have been changed to center the 43 MHz oscillator control voltage. Record this value before changing it back to the default value.			
Note 2. The default crystal aging value (3500) may have been changed to set the 10 MHz reference crystal oscillator frequency. Record this value before changing it back to the default value.			
Note 3. Tune A and/or Tune B may have been changed from the default value to improve the uncorrected output of the exciter. Record the existing Tune A and B values before changing them. The default values of Tune A and B can be restored by pressing the Reset Tuning soft key on the Up Converter Diagnostics screen.			

5.4 Typical Settings for the More Critical Exciter Setups

Some of the critical setups, which can have a large effect on exciter and transmitter operation, are given in Table 5-2. The remainder of the exciter setups should be fairly obvious when viewing the various setup screens. For additional information concerning the exciter setup screens, see Section 3.6, Details of the System Setup Screens, on page 3-27.

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Table 5-2 Typical Settings For Some of the More Critical Exciter Setup Functions

Setup Screen and location in Technical Manual	**Function**	**Typical Setting**
Exciter Setup (screen 1 of 2) Section 3.6.1, Exciter Setup Screens, on page 3-28	Channel	Set to correct channel
	Frequency Offset	Set to 0 or required offset in Hz
	SMPTE Test Pattern Note: SMPTE 310 input is active when OFF is selected and blocked for any other selection.	OFF, if SMPTE 310 is present at exciter input, or any pattern (except loopback) if SMPTE 310 is not present.
	Waveguide Provides group delay precorrection to compensate for waveguide group delay.	None, if waveguide group delay precorrection is not required. Select waveguide type and enter length if waveguide group delay precorrection is required.
Exciter Setup (screen 2 of 2) Section 3.6.1.1, Exciter Setup Screen 2 of 2, Power Limit and Calibration, on page 3-30	Power Limit	Limits maximum exciter power output (or transmitter power output, if exciter is used to control transmitter output power)
RTAC Setup Section 3.6.2, RTAC Setup Screen, on page 3-32	Filter Type: **Use Standard** if the standard D-Mask filter is used. **Use Asymm** (asymmetrical) if the sharp tuned filter (sometimes called “Cool Fuel”) is used or if the group delay for the transmitter is not symmetrical, such as when its output is reflected through an adjacent channel sharp tuned filter in order to combine the two transmitters. **Use CH 14 Super** only if the system includes a special high power filter used to protect land mobile operators on frequencies immediately below ch 14. **Exciter must be restarted** to make filter change active.	
	Max. Peak Stretch (prevents nonlin correction peaks form over driving solid state amps).	3db (may be set lower on some transmitters.)
	Off Air Mode (choices are Hold or Bypass)	Hold
Display	Chart Source (exciter spectrum analyzer display input)	Tx Post HPF
External I/O Section 3.6.4, External I/O Setup Screen, on page 3-35	VSWR Foldback Threshold (low limit)	0.25 Vdc, see Note 1
	VSWR Foldback Threshold (high limit)	5.0 Vdc, see Note 1
	VSWR Foldback (max RF power reduction)	50% of normal exciter output power, see Note 1
	RF Cutoff (exciter output power level at which control logic switches to backup exciter)	50% of the normal exciter output power.
Note 1. Some transmitters use this feature for the transmitter output system VSWR foldback and other transmitters use a separate circuit for VSWR foldback. Consult the transmitter technical manual for instructions concerning VSWR foldback system and setup.		

5.5 Exciter Troubleshooting Flow Charts

The four charts in this section offer some initial troubleshooting guides for the more common setup related problems encountered with the APEX exciter. More detailed troubleshooting information is available in the succeeding sections of this chapter.

All of the exciter setup functions and normal operation instructions as well as many of the diagnostic functions are controlled by the front panel LCD touch screen display. As a result, many of the troubles experienced with the Apex exciter and transmitter RF system will be due to improper exciter touch screen settings.

The following four flow charts are an attempt to guide the user through some of the more typical touch screen involved problems. An attempt was made to structure the charts in a top to bottom and left to right simple to complex format. The four charts include:

Figure 5-6, Pilot Frequency Error Troubleshooting Flow Chart, on page 5-14.

Figure 5-7, Low or No Output Power Troubleshooting Flow Chart, on page 5-15.

Figure 5-8, Transmitter Fails FCC Mask Test Troubleshooting Flow Chart, on page 5-16.

Figure 5-9, Transmitter Has Excessive EVM Troubleshooting Flow Chart, on page 5-17.

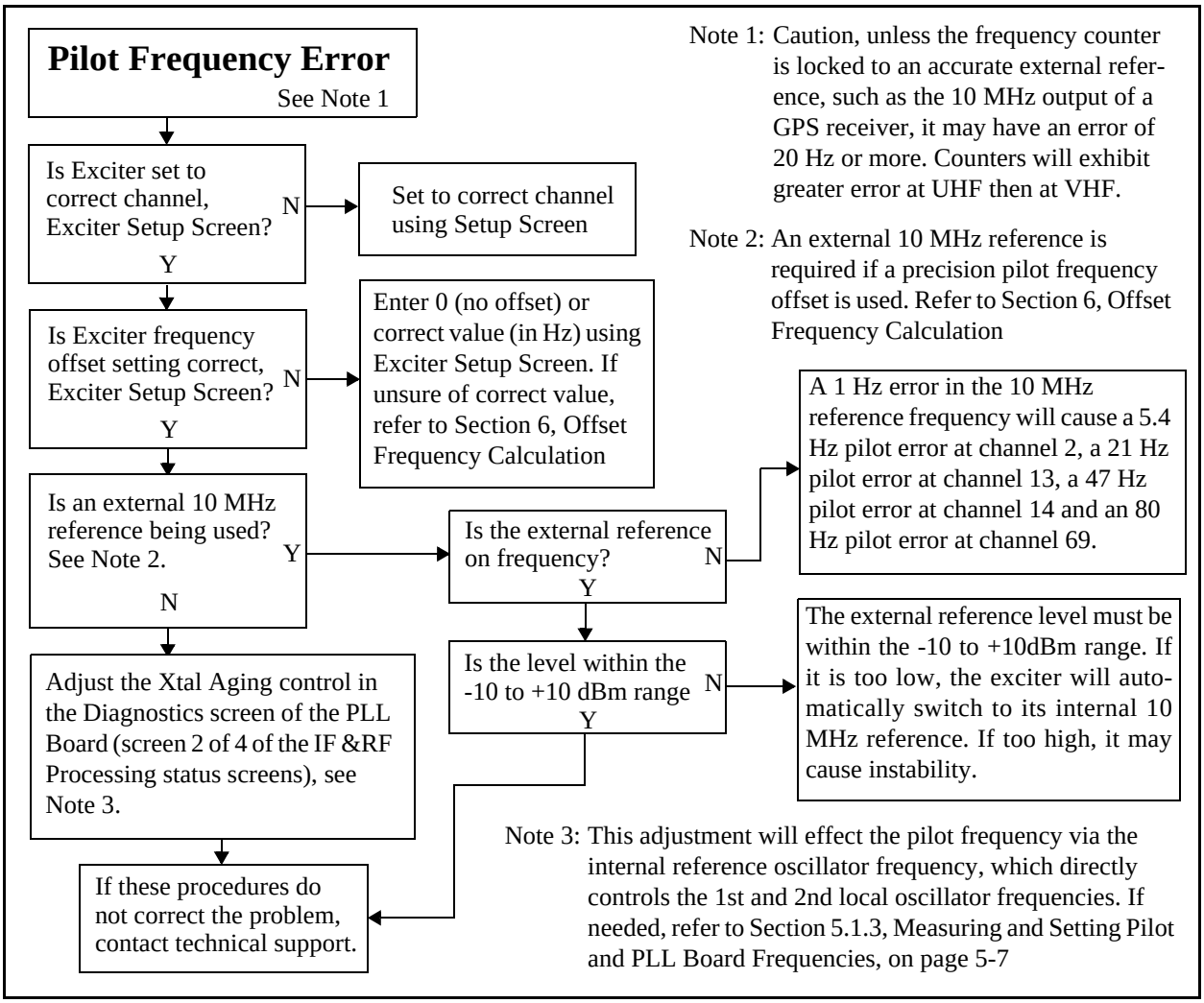
Pilot Frequency Error
See Note 1
Is Exciter set to correct channel, Exciter Setup Screen?
N
Y
Set to correct channel using Setup Screen
Is Exciter frequency offset setting correct, Exciter Setup Screen?
N
Y
Enter 0 (no offset) or correct value (in Hz) using Exciter Setup Screen. If unsure of correct value, refer to Section 6, Offset Frequency Calculation
Is an external 10 MHz reference being used? See Note 2.
Y
N
Is the external reference on frequency?
N
Y
A 1 Hz error in the 10 MHz reference frequency will cause a 5.4 Hz pilot error at channel 2, a 21 Hz pilot error at channel 13, a 47 Hz pilot error at channel 14 and an 80 Hz pilot error at channel 69.
Adjust the Xtal Aging control in the Diagnostics screen of the PLL Board (screen 2 of 4 of the IF &RF Processing status screens), see Note 3.
Is the level within the -10 to +10 dBm range
N
Y
The external reference level must be within the -10 to +10dBm range. If it is too low, the exciter will automatically switch to its internal 10 MHz reference. If too high, it may cause instability.
If these procedures do not correct the problem, contact technical support.
Note 1: Caution, unless the frequency counter is locked to an accurate external reference, such as the 10 MHz output of a GPS receiver, it may have an error of 20 Hz or more. Counters will exhibit greater error at UHF then at VHF.
Note 2: An external 10 MHz reference is required if a precision pilot frequency offset is used. Refer to Section 6, Offset Frequency Calculation
Note 3: This adjustment will effect the pilot frequency via the internal reference oscillator frequency, which directly controls the 1st and 2nd local oscillator frequencies. If needed, refer to Section 5.1.3, Measuring and Setting Pilot and PLL Board Frequencies, on page 5-7

Figure 5-6 Pilot Frequency Error Troubleshooting Flow Chart

WARNING: Disconnect primary power prior to servicing.

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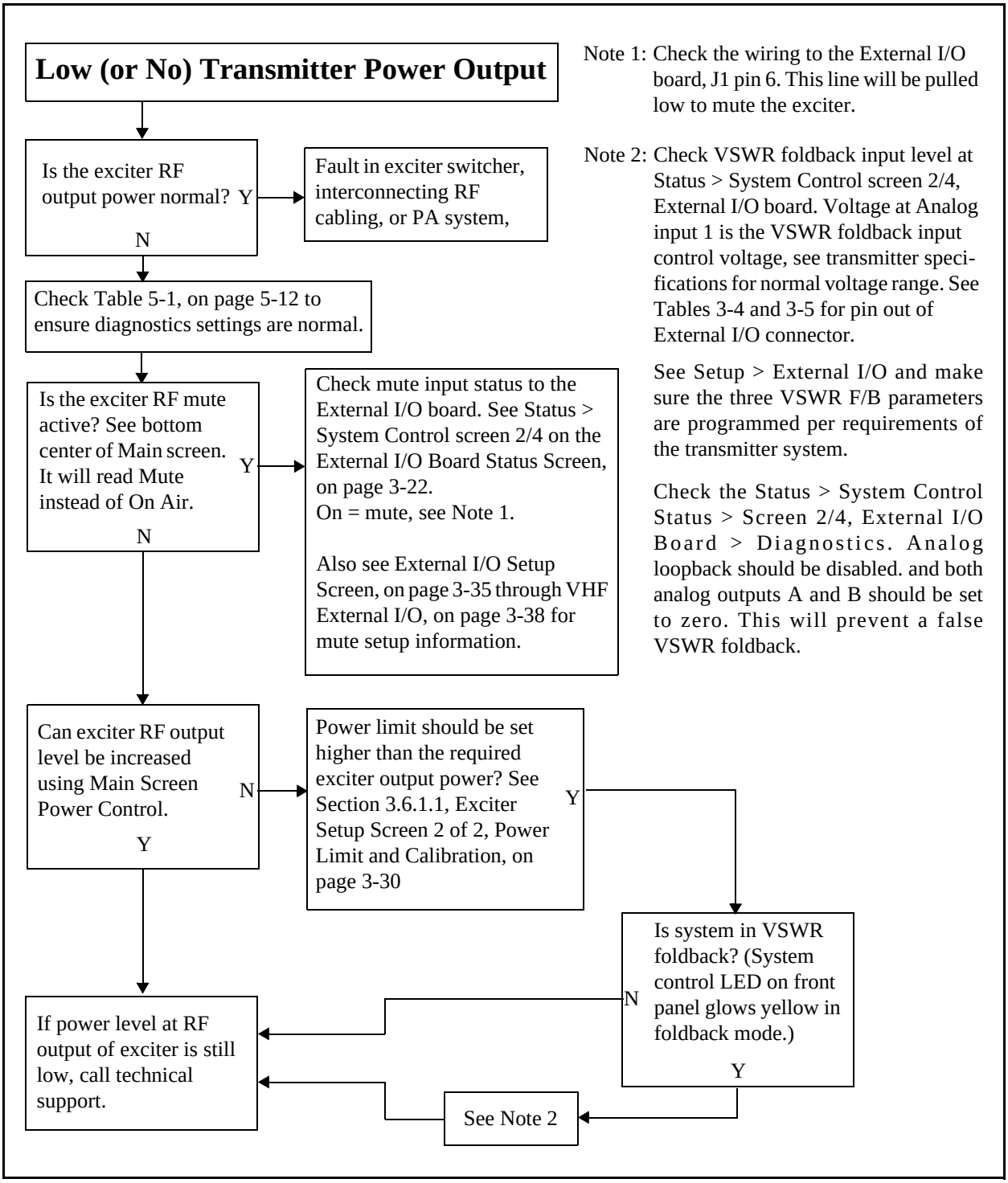
Low (or No) Transmitter Power Output
Is the exciter RF output power normal?
Y
N
Fault in exciter switcher, interconnecting RF cabling, or PA system,
Check Table 5-1, on page 5-12 to ensure diagnostics settings are normal.
Is the exciter RF mute active? See bottom center of Main screen. It will read Mute instead of On Air.
Y
N
Check mute input status to the External I/O board. See Status > System Control screen 2/4 on the External I/O Board Status Screen, on page 3-22.
On = mute, see Note 1.
Also see External I/O Setup Screen, on page 3-35 through VHF External I/O, on page 3-38 for mute setup information.
Can exciter RF output level be increased using Main Screen Power Control.
N
Y
Power limit should be set higher than the required exciter output power? See Section 3.6.1.1, Exciter Setup Screen 2 of 2, Power Limit and Calibration, on page 3-30
Y
Is system in VSWR foldback? (System control LED on front panel glows yellow in foldback mode.)
N
Y
If power level at RF output of exciter is still low, call technical support.
See Note 2
Note 1: Check the wiring to the External I/O board, J1 pin 6. This line will be pulled low to mute the exciter.
Note 2: Check VSWR foldback input level at Status > System Control screen 2/4, External I/O board. Voltage at Analog input 1 is the VSWR foldback input control voltage, see transmitter specifications for normal voltage range. See Tables 3-4 and 3-5 for pin out of External I/O connector.
See Setup > External I/O and make sure the three VSWR F/B parameters are programmed per requirements of the transmitter system.
Check the Status > System Control Status > Screen 2/4, External I/O Board > Diagnostics. Analog loopback should be disabled. and both analog outputs A and B should be set to zero. This will prevent a false VSWR foldback.

Figure 5-7 Low or No Output Power Troubleshooting Flow Chart

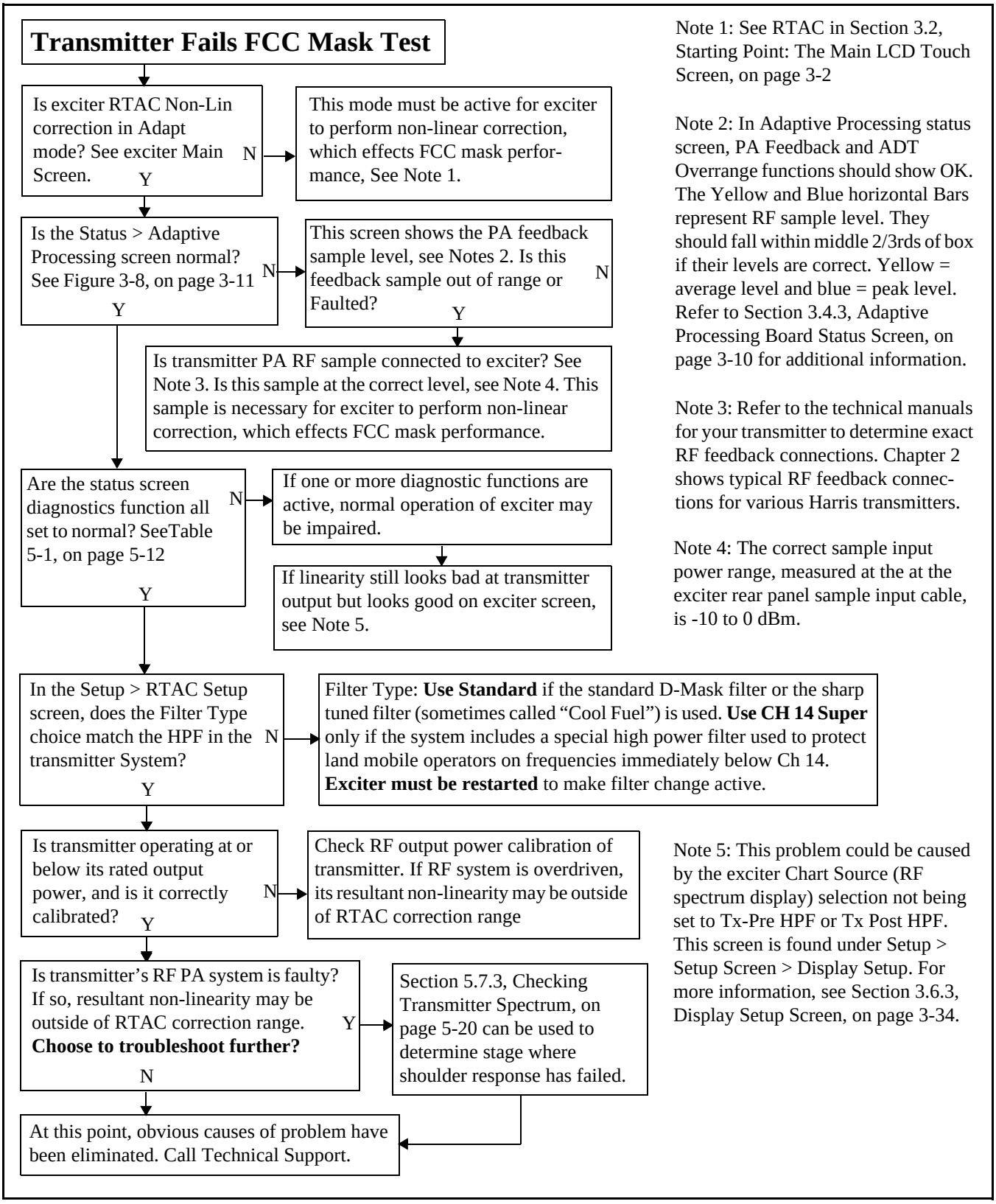
Transmitter Fails FCC Mask Test
Is exciter RTAC Non-Lin correction in Adapt mode? See exciter Main Screen.
N
Y
This mode must be active for exciter to perform non-linear correction, which effects FCC mask performance, See Note 1.
Is the Status > Adaptive Processing screen normal? See Figure 3-8, on page 3-11
N
Y
This screen shows the PA feedback sample level, see Notes 2. Is this feedback sample out of range or Faulted?
N
Y
Is transmitter PA RF sample connected to exciter? See Note 3. Is this sample at the correct level, see Note 4. This sample is necessary for exciter to perform non-linear correction, which effects FCC mask performance.
Are the status screen diagnostics function all set to normal? SeeTable 5-1, on page 5-12
N
Y
If one or more diagnostic functions are active, normal operation of exciter may be impaired.
If linearity still looks bad at transmitter output but looks good on exciter screen, see Note 5.
In the Setup > RTAC Setup screen, does the Filter Type choice match the HPF in the transmitter System?
N
Y
Filter Type: Use Standard if the standard D-Mask filter or the sharp tuned filter (sometimes called "Cool Fuel") is used. Use CH 14 Super only if the system includes a special high power filter used to protect land mobile operators on frequencies immediately below Ch 14. Exciter must be restarted to make filter change active.
Is transmitter operating at or below its rated output power, and is it correctly calibrated?
N
Y
Check RF output power calibration of transmitter. If RF system is overdriven, its resultant non-linearity may be outside of RTAC correction range
Is transmitter's RF PA system is faulty? If so, resultant non-linearity may be outside of RTAC correction range. Choose to troubleshoot further?
Y
N
Section 5.7.3, Checking Transmitter Spectrum, on page 5-20 can be used to determine stage where shoulder response has failed.
At this point, obvious causes of problem have been eliminated. Call Technical Support.
Note 1: See RTAC in Section 3.2, Starting Point: The Main LCD Touch Screen, on page 3-2
Note 2: In Adaptive Processing status screen, PA Feedback and ADT Overrange functions should show OK. The Yellow and Blue horizontal Bars represent RF sample level. They should fall within middle 2/3rds of box if their levels are correct. Yellow = average level and blue = peak level. Refer to Section 3.4.3, Adaptive Processing Board Status Screen, on page 3-10 for additional information.
Note 3: Refer to the technical manuals for your transmitter to determine exact RF feedback connections. Chapter 2 shows typical RF feedback connections for various Harris transmitters.
Note 4: The correct sample input power range, measured at the at the exciter rear panel sample input cable, is -10 to 0 dBm.
Note 5: This problem could be caused by the exciter Chart Source (RF spectrum display) selection not being set to Tx-Pre HPF or Tx Post HPF. This screen is found under Setup > Setup Screen > Display Setup. For more information, see Section 3.6.3, Display Setup Screen, on page 3-34.

Figure 5-8 Transmitter Fails FCC Mask Test Troubleshooting Flow Chart

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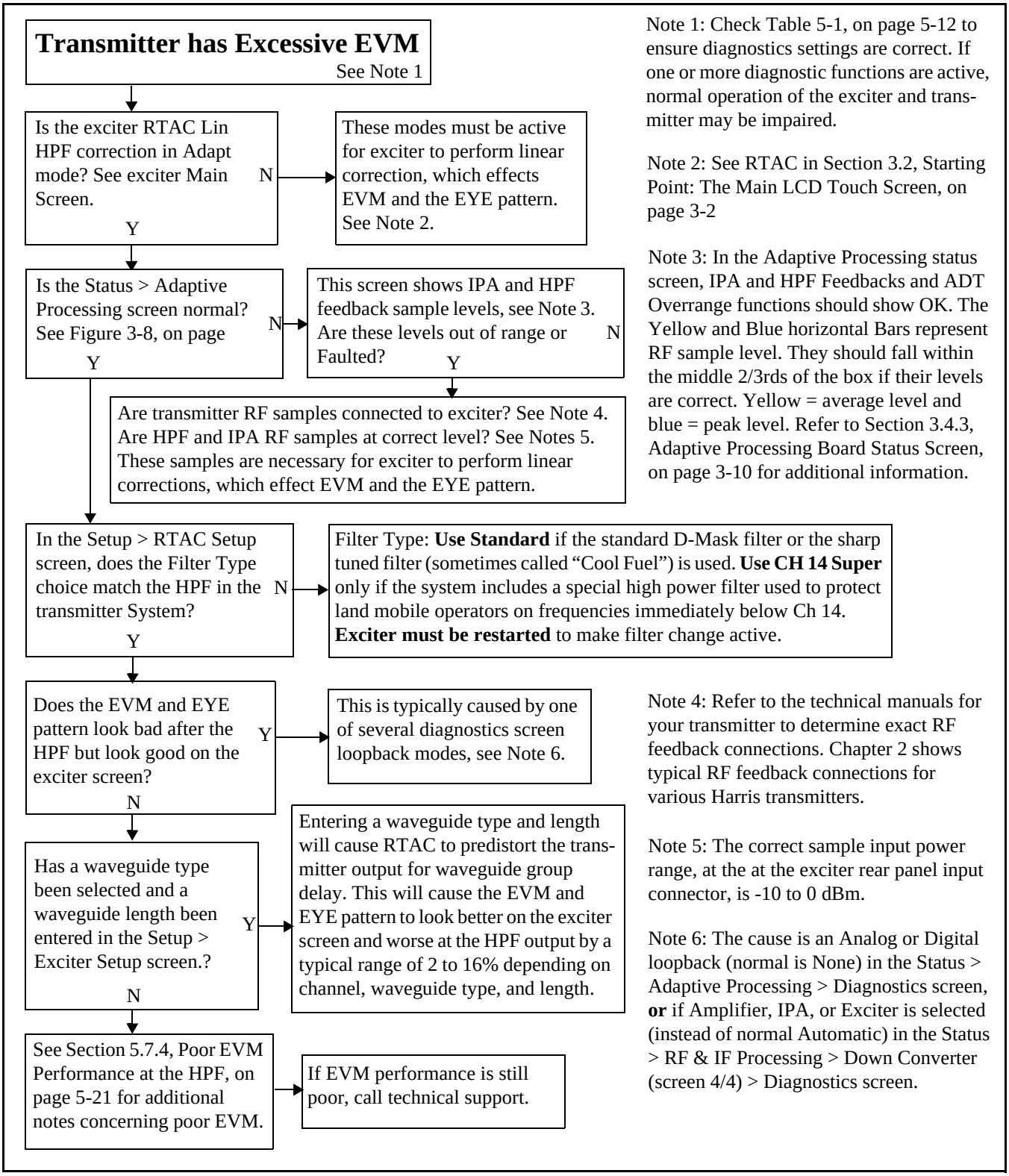
Transmitter has Excessive EVM
See Note 1
Is the exciter RTAC Lin HPF correction in Adapt mode? See exciter Main Screen.
N
Y
These modes must be active for exciter to perform linear correction, which effects EVM and the EYE pattern. See Note 2.
Is the Status > Adaptive Processing screen normal? See Figure 3-8, on page
N
Y
This screen shows IPA and HPF feedback sample levels, see Note 3. Are these levels out of range or Faulted?
N
Y
Are transmitter RF samples connected to exciter? See Note 4. Are HPF and IPA RF samples at correct level? See Notes 5. These samples are necessary for exciter to perform linear corrections, which effect EVM and the EYE pattern.
In the Setup > RTAC Setup screen, does the Filter Type choice match the HPF in the transmitter System?
N
Y
Filter Type: Use Standard if the standard D-Mask filter or the sharp tuned filter (sometimes called "Cool Fuel") is used. Use CH 14 Super only if the system includes a special high power filter used to protect land mobile operators on frequencies immediately below Ch 14. Exciter must be restarted to make filter change active.
Does the EVM and EYE pattern look bad after the HPF but look good on the exciter screen?
Y
N
This is typically caused by one of several diagnostics screen loopback modes, see Note 6.
Has a waveguide type been selected and a waveguide length been entered in the Setup > Exciter Setup screen.?
Y
N
Entering a waveguide type and length will cause RTAC to predistort the transmitter output for waveguide group delay. This will cause the EVM and EYE pattern to look better on the exciter screen and worse at the HPF output by a typical range of 2 to 16% depending on channel, waveguide type, and length.
See Section 5.7.4, Poor EVM Performance at the HPF, on page 5-21 for additional notes concerning poor EVM.
If EVM performance is still poor, call technical support.
Note 1: Check Table 5-1, on page 5-12 to ensure diagnostics settings are correct. If one or more diagnostic functions are active, normal operation of the exciter and transmitter may be impaired.
Note 2: See RTAC in Section 3.2, Starting Point: The Main LCD Touch Screen, on page 3-2
Note 3: In the Adaptive Processing status screen, IPA and HPF Feedbacks and ADT Overrange functions should show OK. The Yellow and Blue horizontal Bars represent RF sample level. They should fall within the middle 2/3rds of the box if their levels are correct. Yellow = average level and blue = peak level. Refer to Section 3.4.3, Adaptive Processing Board Status Screen, on page 3-10 for additional information.
Note 4: Refer to the technical manuals for your transmitter to determine exact RF feedback connections. Chapter 2 shows typical RF feedback connections for various Harris transmitters.
Note 5: The correct sample input power range, at the at the exciter rear panel input connector, is -10 to 0 dBm.
Note 6: The cause is an Analog or Digital loopback (normal is None) in the Status > Adaptive Processing > Diagnostics screen, or if Amplifier, IPA, or Exciter is selected (instead of normal Automatic) in the Status > RF & IF Processing > Down Converter (screen 4/4) > Diagnostics screen.

Figure 5-9 Transmitter Has Excessive EVM Troubleshooting Flow Chart

5.6 General Troubleshooting

This section is a general troubleshooting guide to the APEX exciter.

The digital techniques used in the exciter result in a highly reliable product, but when there is a need to check the exciter or the signal passing through it, much, if not all, of the trouble shooting will be performed through the LCD screens, and perhaps some test equipment.

The following paragraphs describe the levels and indications which may be used to verify proper operation of an APEX exciter or to isolate a possible problem in the unit to a circuit board level. In this chapter, troubleshooting is divided into two categories.

- System Troubleshooting - Problems caused by conditions outside the exciter.
- Exciter Troubleshooting - Problems caused within the exciter.

5.6.1 Troubleshooting Tips

If an exciter problem is suspected, first try to narrow the suspect area to a part of the exciter.

1 Is the exciter powered? Make certain power is applied and the AC power switch is turned on.

The fan, at the rear of the exciter, should be running and the LCD display should be illuminated.

2 If the exciter display is completely dark touch the display to see if it illuminates. The screen saver may have been active. Troubleshooting a dark screen is covered in Section 5.8.2 on page 5-22.

3 Are there any fault indications on the LCD display or front panel LEDs?

A yellow fault display is a warning that a parameter is approaching a limit. A red fault display indicated that the parameter has exceeded its limit.

Touching the flashing fault soft key at the bottom of any screen will switch the display to the status screen for the faulted board, or the System Status screen if faults in more than one board exist. The Various screens of the LCD display should quickly lead to a faulty circuit board.

4 Circuit board operating voltages are listed on most of the status screens. If a voltage on any of the screens is out of tolerance, a red fault indication appears to the right of the voltage indication.

5 Is the RF output at the normal level? The exciter output can be set to any level from 0 to 250 mW average. Each transmitter has its own unique input drive requirement, which should be recorded in the transmitter final test data. If the normal input to your transmitter is not known, it should fall somewhere in this range.

6 If there is no output, check the RF Mute status on the at the bottom of any screen. It will indicate On-Air, Off-Air, or Mute.

If the exciter stays muted when attempting to unmute from the exciter setup screen, check the mute status on the System Control Status 2/4, External I/O Board. If it indicates On, a mute command is being sent to the external I/O board via connector J1

5.7 System Troubleshooting

Some faults that show up on the exciter screen may be systems related. Some of these are covered in this section.

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5.7.1 IPA, PA, HPF, or ADC Adaptive Processing Faults

IPA, PA, HPF, or ADC over range faults on adaptive processing board can be caused by Feedback samples that are too low or too high. The power level for each of these RF feedback samples should fall between -10 to 0 dBm at the rear panel of the exciter. Chapter 2 of this manual gives some typical examples of RF feedback sample arrangements.

5.7.2 Transmitter Response Not Conforming to FCC Mask Requirements

Transmitter spectrum response outside of the FCC Mask limits may be caused by failure of the adaptive correction system in the exciter, but it may also be caused by transmitter system problems outside of the exciter. It should be noted that poor adjacent channel spectral response is caused by inter modulation products which are caused by poor PA linearity. Some of these are listed below.

- Over driving, to the point of clipping, of low level stages prior to IPA (or driver).

  If an amplifier is driven to clipping, non linear correction beyond that point is not possible.

- Poor linearity of stages prior to the PA (or driver).

  If two successive amplifiers are both fairly non linear, and especially if they have different non linearity curves, correction at the output of the PA will be difficult if not impossible. This leads to the idea that the amplifiers prior to the driver (or IPA) must be very linear and have good head room, with shoulders that are -50 dB with respect to the response at the center of the channel before RTAC is activated.

  In the case of IOT transmitters, the IPA should be linearized and have a shoulder response of -45 dB with respect to the response at the center of the channel before RTAC is activated.

  On the adaptive processing status screen, excessive peak (blue bar) to average (yellow bar) ratio of the IPA and/or PA samples indicate large values of corrections are being used.

- Excessively poor PA linearity.

- PA input tuning too narrow (for IOT transmitters). Input tuning should have a bandwidth of 12 MHz minimum and 18 MHz ideal.

  In order to cancel the adjacent channel inter modulation products generated by the PA, the pre correction signal must include inter modulation products of the same frequency which are 180 degrees out of phase with the PA generated products. If the PA input tuning is too narrow, the amplitude and/or phase of some of the adjacent channel pre distortion signal components may be changed, or they may be eliminated.

- Improper PA output tuning (for IOT transmitters) - wrong amount of saddle or bandwidth effects linearity and gain.

  These tuning errors cause the load impedance presented to the IOT to change, which can greatly effect the linearity of the PA. If the PA becomes too non linear, it may get beyond the correcting range or the RTAC non linear corrector.

- For IOT transmitters, poor PA linearity caused by improper idle current may push the PA linearity beyond the correcting ability of the RTAC system. Idle current is determined by the PA bias. This problem is more common in IOT transmitters, because idle current is often set at the factory for solid state transmitter PA modules.

  The solution is to set the RTAC correction to bypass and adjust the PA bias for best adjacent channel shoulder response. After this adjustment, check the idle current to make sure it is within the IOT manufacturer's specifications.

- Non-linearities in RF feedback sample path. This causes the exciter to correct for them along with the transmitter non-linearities. In this case, the exciter response display would appear to be within specifications but the test equipment connected to the transmitter would indicate that the system was not within specifications.

5.7.3 Checking Transmitter Spectrum

The spectrum analyzer display on the main screen of the exciter can be used to view the spectral response at the outputs of the various stages within the transmitter PA system and within the exciter. The process is as follows.

1 On the main screen, in the RTAC section (lower left side), set the Lin IPA, Lin HPF, and Non Lin functions to Bypass to disable RTAC correction.

2 In the Setup > Display screen, the Chart Source selections can be used to cause the main screen spectrum analyzer to monitor the indicated locations in the exciter and PA system. The Chart Source choices and their sources are listed below.

   Tx-Post HPF: RF sample taken after the high power (FCC Mask) filter.

   Tx-Pre HPF: RF sample taken after the transmitter PA but before the high power (FCC Mask) filter.

   IPA: RF sample taken at the output of the transmitter IPA.

   Exciter: RF sample taken at the output of the exciter one-watt output amplifier.

   8VSB w/RTAC: Digital signal taken at output of adaptive precorrector board. The DAC board follows next.

   C, D, and J represent memories at various locations (from input to output) on the Adaptive Precorrector board.

   BIT: Digital signal taken at modulator board to adaptive precorrector board interface.

   8VSB Ref: Digital signal obtained at the output of the modulator board.

3 With the RTAC correction bypassed and the transmitter operating at 100% power, the shoulder response should be as follows:

   A After the transmitter PA, they should be in the range of 28 to 36 dB below the response at the center of the channel.

   B At the output of the IPA, the shoulders should look a few dB better then the output of the PA, and will probable fall within the 32 to 38 dB range.

   C At the output of the exciter, and any point within the exciter, the shoulders should be 50 to 55 dB below the response at the center of the channel.

   If the shoulder response at and before the output of the exciter is not at least 50 dB below the response at the center of the channel, the exciter is not operating properly.

4 When RTAC is operating, it is precorrecting for the transmitter IPA and PA non-linearities, therefore, the shoulders at the output of the PA should look best and be 38 dB or more below the response at the center of the channel. Before the PA, the shoulders will not look as good due to precorrection of the signal.

5.7.4 Poor EVM Performance at the HPF

Poor EVM performance at HPF output may be caused by failure of the adaptive correction system in the exciter, but it may also be caused by transmitter system problems outside of the exciter. Some of these are listed below.

- VSWR in RF sample feedback path, causing the exciter to correct for them along with the transmitter linear distortions. In this case, the exciter EVM and EYE display would appear to be within specs.
- Pre distortion for waveguide group delay, caused by selecting a type and length of waveguide in the exciter setup screen. This pre distortion is intended to produce good EVM at the output of the waveguide run. The problem would show up on test equipment which is connected to the output of the high power filter, but would not show up on the exciter main screen on-air data or eye display since this pre distortion is subtracted out of the exciter main screen displays.

  Waveguide group delay predistortion typical ranges from 2 to 16% depending on channel, waveguide type, and length.
- Noise or RF signal pickup due to a faulty HPF sample feedback cable.

5.7.5 MPEG Faults

The input signal to the exciter is the ATSC transport signal in the SMPTE 310M format. Faults on the MPEG Input status screen could be caused by a faulty input transport stream.

If the quality of the input signal is suspect, a bitstream analyzer should be used to analyze it, or a known good SMPTE 310M transport signal source should be connected to the SMPTE 310 M input of the exciter.

If an MPEG input fault exists, check the input signal strength on the MPEG Input Status screen. Below 50% causes a fault.

This input will show fault with a valid SMPTE 310M input to the exciter if a SMPTE Test Pattern is selected from the Exciter Setup screen.

5.8 Exciter Troubleshooting

5.8.1 Pilot Frequency Error

When not using an external 10 MHz reference, the internal 10 MHz reference oscillator in the PLL board ultimately determines accuracy of the pilot frequency at the output of the exciter.

Pilot frequency accuracy is dependant on the accuracy of the 1st and 2nd local oscillators (LOs) in the PLL board, which get their reference from the 10 MHz reference oscillator. If a large pilot frequency error exists, check the PLL status screen (second of four IF & RF processing status screens). On this screen, the supply voltages should be within tolerance (they will show a red fault or yellow warning if not in tolerance). Also check the status of the IF PLL Lock (1st LO) and RF PLL Lock (2nd LO). They should both be locked. The 10 PLL Lock status will be yes (locked) if an external reference is present (screen indicates yes) and no if it is absent.

If a fault exists in one or more of the PLLs and the power supply voltages are ok, a board replacement should be tried.

If one or more of the supply voltages show warnings or faults, the problem may be on the PLL board, UDC interface board, or power supply. Refer to Section 5.8.3 for additional power distribution trouble shooting information.

5.8.2 Dark Screen

This problem assumes that the AC power is present, the power switch is on, and the fan is operating.

The exciter display is completely dark and touching the display will not cause it to illuminate (screen saver check) perform the following:

Note

The front panel display is controlled by the controller board (A8) and the front panel display board (A10).

1 Check for the presence of supply voltages on the controller board by observing the following LEDs.

DS4 (green) indicates presence of +5 Vdc supply and DS1 (green) indicates the on board regulator is producing +3.3 Vdc. DS2 (red) indicates a 3.3 Vdc fault when illuminated. Further power supply voltage checks can be made by referring to Section 5.8.3, Power Supply Voltages on page 5-23.

2 Change the controller and/or the display boards.

A faulty controller board may be the cause of a bad front panel display. If LEDs 0 through 7are scrolling, the fault is probably a cable going to the front panel board or the board itself. If they are not scrolling, and the controller board power supplies are ok, change the controller board.

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5.8.3 Power Supply Voltages

Circuit board operating voltages are listed on most of the status screens. If the voltages on these screens are out of tolerance, a red fault indication appears to the right of the voltage indication.

If one or more of the +5, +15, or -15 volt supplies are faulted on more than one board, or if the display is dark and cannot be illuminated by touching it, the regulated power supplies in the top (analog) side of the exciter should be checked.

The power supply voltages are listed in Table 5-3.

Warning

Removal of the plastic shield which covers the exciter power supply and fan exposes 120 Vac to the technician. Therefore, proper procedure for measuring voltages in the following paragraphs requires prior removal of all power before the plastic shield is removed from the analog tray. The test meter is to be located outside the shield and the plastic shield replaced prior to applying power.

All of the power supply voltages can be accessed by removing the top cover of the supply.

- The three 15 volt supplies can be measured at J4 of the UDC Interface board or at SK2 of the power supply, refer to Table 5-3 for the pin numbers.
- The 5 volt supply can be measured at J6 of the controller board (bottom side of the exciter) or at SK3 of the power supply, refer to Table 5-3 for the pin numbers.

A short in the wiring or in one of the circuit boards could cause a supply voltage to fold back (to zero volts). This can be checked by unloading the supply one circuit board at a time.

If the supply is totally dead, follow all precautions listed in the warning above and check the fuse located in the power supply input filter assembly.

Table 5-3 Exciter Power Supply Voltages

Voltage	Use	Tolerance	PS Jack and Pin	Destination Jack and Pin
+5 Vdc	Power for digital tray		SK3 pin 2	Controller, J6 pins 10 - 13
Common for +5 V			SK3 pin 1	Controller, J6 pins 1 - 4
+15	Power for analog tray		SK2 pins 1 - 2	UDC Interface, J4 pins 1 - 2
-15	Power for analog tray		SK2 pin 6	UDC Interface, J4 pin 6
Common for +/- 15 Vdc			SK2 pins 3 - 5	UDC Interface, J4 pins 3 - 5
+15 Vdc Float	Fan power		SK2 pin 8	UDC Interface, J4 pin 8
Common for +15 Vdc Float			SK2 pin 9	UDC Interface, J4 pin 9

5.8.4 Troubleshooting Down to the Board Level

Isolating a defective circuit board is relatively easy if the faults appear on one or more of the status screens. This involves interpreting the faults so that they point to a particular board. Details of the status screens and their faults are covered in Section 3.4 on page 3-8.

Occasionally, the exciter RF output parameters will not meet specifications and the status screen faults will not point to a particular board. Troubleshooting these types of problems down to the board level can be more challenging. Such problems can include, but are not limited to, low or zero RF output power, irregular spectral response, or EVM and EYE pattern. These types of problems require on screen and off screen signal tracing, which requires a knowledge of the signal path through the exciter. A brief signal path review is given in the next two headings.

5.8.4.1 Digital Tray Transmission Data Path

See Figure 5-2, on page 5-3, the digital tray layout diagram and Figure 4-3, on page 4-7 for a signal flow block diagram of the APEX exciter. The signal enters the SMPTE board, then goes to the modulator board. From the modulator board, it travels through the controller board to the adaptive precorrector board. From there it goes to the DAC board, the output of which is the 10.762 MHz first IF signal. The first IF signal goes to the input of the up converter board in the analog tray.

5.8.4.2 Analog Tray Signal Path

See Figure 4-3, on page 4-7 for a signal flow block diagram of the APEX exciter and Figure 5-1, on page 5-2 for the analog tray layout diagram. The IF signal enters the up converter board, the output of which goes to the output amplifier. The output of the output amplifier goes to the transmitter PA(s) and a sample of the output is connected to the input multiplexer of the down converter board, along with the other three transmitter system feedback samples. The output of the down converter board is connected to the input of the ADC board.

5.8.5 Isolating Problem to the Analog or Digital Tray

Three internal loopback functions are available to help isolate problems to the digital or analog tray. They are the analog and digital loopback features of the adaptive processing diagnostics screen, used to determine the health of the digital tray, and the exciter loopback feature of the down converter board diagnostics screen, used to determine the health of the entire exciter (digital and analog trays).

After determining which tray has a problem, isolating the defective board in that tray will be discussed.

5.8.5.1 Checking Operation of the Entire Digital Tray

Two methods are available to verify correct operation of the entire digital signal processing tray. The first method excludes the DAC board, the ADC board, and the analog tray, and the second method only excludes the analog tray.

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While performing these tests alternately monitor exciter and 8VSB w/RTAC on the main screen chart display (these are selected in the chart source on the display setup screen). The exciter display is derived from the ADC data output and the 8VSB W/RTAC display is derived from the DAC input data.

1 This method uses the digital loopback feature of the adaptive processing diagnostics screen. It loops the digital input of the DAC to the digital output of the ADC (J1 to J2 on the Adaptive corrector board), which eliminates the two converters and the entire analog tray from the test.

   A When viewing the digital loopback main screen monitoring displays, the EYE pattern and spectral response should look good.

   B Observing the On-Air Data, the LSB and USB (lower and upper sidebands) should be better than -55 dB.

   The SNR and EVM readings will show N/A until the Lin HPF of the main screen RTAC is set to adapt, at which time the SNR should be better then 32 dB and the EVM should be better the 2%,

2 This method uses the analog loopback feature of the adaptive processing diagnostics screen. It loops the 10.762 MHz analog IF output of the DAC to the analog IF input of the ADC and bypasses the analog IF input from the down converter. This eliminates the entire analog tray from the test. The analog loopback is accomplished via cable W26, which connects J2 of DAC to J2 on ADC.

   A When viewing the analog loopback main screen monitoring displays, the EYE pattern will not look good unless the Lin HPF of the main screen RTAC is set to adapt. Observing the main screen On-Air Data, the SNR should be better then 32 dB and the EVM should be better than 2%, and the LSB and USB (lower and upper sidebands) should be better than -50 dB.

   The chart source Post HPF, Pre HPF, IPA, and Exciter selections all come from the ADC digital output (as that particular source is being monitored). Since only the exciter output is being looped back in this test, all of these selections will display the exciter output.

Faulty DAC and/or ADC boards are indicated if the exciter passed the digital loopback test and failed the analog loopback test.

5.8.5.2 Checking Operation of the Entire Exciter

It is possible to view the output of the exciter on the main screen to verify its overall correct operation. This test loops an RF sample from the output of the output amplifier through the down converter to the ADC board. The output of the ADC is monitored on the main screen EYE pattern, spectral response and On-Air data displays. The procedure is given below.

1 In the down converter board diagnostics screen, set the RF sample select from automatic to exciter. This causes the RF sample from exciter output to be the only signal that is looped back through the down converter.

2 Set the main screen chart source (on the display setup screen) to the Exciter position. This monitors the output of the ADC.

   Actually, the chart source Post HPF, Pre HPF, IPA, and Exciter selections all come from the ADC digital output (as the particular source is being monitored). Since the exciter output is the only signal which is looped back during this test, all of the four chart source selections mentioned above will display the exciter output.

3 Set RTAC Lin HPF to adapt.

4 The EVM should be below 2.8%, the SNR should be 32 dB, and the upper and lower sideband attenuation should be 50 dB or better.

If the above test is passed and the front panel indicates output power (exciter not muted) but no power is present at exciter rear panel output connector, the problem could be with the output amplifier mute circuit, the UDC board mute circuit or cable W3, which connects the amplifier output connector J2 to the RF output connector on the exciter rear panel. Since the RF sample for the above mentioned test is taken from the output of the output amplifier, the fact that the test was successful and the front panel indicated the presence of output power proves that the amplifier was operating up to the RF sample and detector outputs. Refer to Figure 4-10, on page 4-16, for a block diagram of the output amplifier.

The amplifier mute circuit operates a relay which connects the amplifier output to connector J2 (RF output) on the amplifier board when not muted and connects the amplifier output to connector J3 (RF load) when muted. The mute signal comes in at amplifier connector J5 pin 7, unmuted = +4 Vdc and muted = 0 Vdc.

5.8.6 Isolating a Faulty Board in the Digital Tray

Isolating a faulty board in the digital tray involves checking the status screens of the boards for faults, knowing which board diagnostics screen functions to use, and knowing how to monitor the DTV signal flow through the boards. Each board in the digital tray is discussed below.

5.8.7 SMPTE Board

SMPTE board problems can be divided into the following three general areas.

1 A valid SMPTE 310M signal must be present at the input of the board.

If an MPEG input fault exists, check the input signal strength on the MPEG Input Status screen. Below 50% causes a fault.

The SMPTE input lock of the MPEG Input Status screen will show fault with a valid SMPTE 310M input to the exciter if the SMPTE test pattern selection of the Exciter Setup screen is set to anything but off.

If the quality of the input signal is suspect, a bitstream analyzer should be used to analyze it, or a known good SMPTE 310M transport signal source should be connected to the SMPTE 310 M input of the exciter.

2 Proper output signal must be obtained from the board.

This can be monitored on the main screen chart display by selecting BIT from the chart source options of the display setup screen.

3 Internal board faults.

The operation of the SMPTE board is monitored continuously by the 43MHz Control, Signal Strength, SMPTE Input Lock, and the SMPTE Output Lock. on the MPEG Input Status screen. This screen also displays the 3.3 and 5 Vdc board power voltages. These should direct the user to a potentially faulty input board.

WARNING: Disconnect primary power prior to servicing.

5.8.7.1 Modulator Board

The input transport stream comes from the SMPTE board. Data leaves Modulator board as a 32 bit complex baseband signal. It goes through the controller board and to the adaptive precorrector board. The controller board samples this throughput data and saves it in the BIT memory.

If the transport stream is missing, the modulator board will still put out a signal with null packets. To determine if the modulator board is putting out a transmission stream, do the following.

1 Select display setup > chart source > BIT.

2 On main screen, check the BIT memory (selected from the chart source of the display setup screen) for a correct 8VSB spectrum. The pilot will always appear on the lower side of the spectrum, even though the spectrum will be reversed on some memory displays if channels 2 through 13 are used.

   A The BIT memory is on the controller board. This display should be the same as the 8VSB Ref memory.

   B The 8VSB Ref memory is located at the input of the Adaptive precorrector board.

5.8.7.2 Adaptive Precorrector Board

This board uses several main screen chart memories, selected from the chart source of the display setup screen. They are listed below.

The 8VSB Ref memory is located at the input of the Adaptive precorrector board.

The 8VSB w/RTAC memory monitors the output of the board. This is the signal that drives the DAC to produce the 10.762 MHz 1st IF.

Three intermediate memories are collected as the signal travels through the board. They are used for adaptive processing. In the order of travel (from input to output) they are the C, D, and J memories. Due to pre compensation applied to the signals, the displays from these memories and the 8VSB w/RTAC memory may appear distorted. If all three RTAC samples (on the main screen) are put is Bypass mode, the signals should appear similar to the 8VSB Ref memory signal.

5.8.7.3 ADC and DAC Boards

Troubleshooting defective ADC or DAC boards is covered in Section 5.8.5.1, Checking Operation of the Entire Digital Tray, on page 5-24.

5.8.7.4 Front Panel Board

Troubleshooting a defective front panel board is covered in Section 5.8.2, Dark Screen, on page 5-22.

5.8.7.5 Controller Board

A faulty controller board may be indicated by a bad front panel display. If the front panel display is operating, the controller board status screen can be checked. This is the first screen of the four system control status screens.

1 Check for front panel display and LEDs. If no activity, check the controller board.

2 Controller board has two green LEDs for the dc power. DS1 = +3.3 Vdc and DS4 = +5Vdc.

3 If LEDs 0 through 7 are scrolling, the fault is probably a cable going to the front panel board or the board itself.

   A If the LEDs are not scrolling, check the +5 volt power to board at test point 10 and the +3.3 volt power at test point 5. If the +5 Vdc voltage is valid, replace the board.

5.8.8 Analog Tray Troubleshooting.

A brief outline of troubleshooting topics is included below. The RF input and output levels for the analog tray are listed in Table 5-4.

- Exciter loopback test.

  Loopback tests are covered in Section 5.8.5, Isolating Problem to the Analog or Digital Tray, on page 5-24.

- Pilot frequency test.

  Pilot frequency topics are covered in Section 5.1.3, Measuring and Setting Pilot and PLL Board Frequencies, on page 5-7 and in Section 5.8.1, Pilot Frequency Error, on page 5-22.

- Check dc supply voltages to each board.

  Power supply topics are covered in Section 5.8.3, Power Supply Voltages, on page 5-23 and in Section 4.5.3, Analog Deck Power, on page 4-19.

- Output power level (check power calibration). Power calibration is covered in Section 3.6.1.2 on page 3-31.

- Measuring signal levels and signal frequencies at the inputs and outputs of each board.

  See Table 5-4 for a list of input and output signal levels.

  Analog board frequency measurements are covered in Section 5.1.3 on page 5-7.

  Digital board frequency measurements are covered in Section 5.1.2 on page 5-7.

- Measuring the AM and PM noise of the 10.762 MHz digital tray clock output and CW signal outputs of the PLL board. If an external 10 MHz reference is used, do the output signal measurements with and without it.

- Observe the Spectral response, EYE pattern, and EVM at the DTV signal inputs and outputs of each board. with all three RTAC samples set to bypass.

Table 5-4 Analog Tray RF Input and Output levels

Board	Function and Connector	Level
PLL	First local oscillator output, J9 and J10	+10 dBm +3/-1 dB
	Second local oscillator output, J5 and J6	+10 dBm +3/-1 dB
	External 10 MHz reference input, J3	-10 to +10 dBm
	10.762 MHz clock (from SMPTE board), J7	1.35 V min to 3.15 V max
Up converter	On channel RF output level, J14	-63 to -6 dBm
	10.752 MHz first IF input, J4	+10 dBm peak +/-0.3 dB using two tone test
Output Amplifier	On channel RF output level, J2	26 to 30 dB gain, Up to 250 mW average power
	On channel RF output sample (to down converter), J4	-10 to 0 dBm
Down converter	10.762 MHz output (to ADC board), J5	-10 to -5 dBm
	Exciter input J4, IPA input J3, PA input J2, HPF input J1	Each input is -10 to 0 dBm

5.9 Technical Assistance

If a problem persists, contact Harris Customer Service for advice at 217 222 8200.

6 Offset Frequency Calculation

6.1 Introduction

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The operating frequency of the Harris APEX exciter is set in the Main screen > Setup > Exciter Setup screen by touching the Channel soft key and entering the channel number.

A Pilot offset (if required) is entered by toughing the Exciter Setup screen Freq. Offset soft key and entering the required offset frequency in Hz. Pilot frequency offsets up to +/_ 50kHz can be entered.

This section provides information on how to calculate the three standard pilot frequency offsets.

6.1.1 Offset Pilot Frequency Operation

Many DTV stations will need to use an offset pilot frequency to minimize interference from or to another TV station, on the same channel or on an adjacent channel. Examples of channel assignments which can call for use of an offset are:

- A co-channel DTV transmitter with an area of signal overlap.
- A co-channel NTSC transmitter with signal area overlap.
- An NTSC transmitter on the lower adjacent channel within 88 km of the DTV transmitter site.

  Frequency offsetting is used to place an interfering signal at a frequency where the interference will be less visible, or where it will have a lessened effect. Many NTSC stations are assigned +10 or -10 kHz offsets for this purpose.

If no offset is applied, the pilot is located 2.69055944058 MHz below the channel center frequency and 0.3094405594 MHz above the lower channel edge.

6.1.1.1 DTV transmitters with Lower-Adjacent NTSC

Any DTV station with a lower adjacent channel NTSC transmitter within 88 km must use a specified offset frequency for its pilot. (In some cases, DTV stations may also need to provide this protection for LPTV stations.) Check current FCC Rules and your authorization before applying this offset.

The frequency offset must place the DTV pilot frequency 5.082138 MHz +/-3 Hz higher than the NTSC Visual Carrier frequency. Since the frequency tolerance of the offset is +/-3 Hz, it is essential that both stations use precise frequency control.

6.1.1.1.1 Possible NTSC Frequency Offsets

NTSC stations may have a +/-10 kHz offset to minimize NTSC to NTSC co-channel interference within their grade B signal overlap zones. To further minimize the overlap interference, the offset NTSC stations may have their visual carriers precisely controlled to a specific frequency, such as 10010 Hz or 10,489.51 Hz above or below the non-offset NTSC station.

WARNING: Disconnect primary power prior to servicing.

6.1.1.1.2 Offset Calculation Procedure

Since the DTV pilot frequency is based on the NTSC visual carrier frequency, and the tolerance is +/-3 Hz, any pilot frequency calculation for this situation must start with the Visual carrier frequency of the NTSC station. The following procedure can be used.

1 Determine the exact visual carrier frequency (F_V) for the NTSC transmitter.

2 Calculate the offset pilot frequency (F_{PO}) using the following formula.

$$F_{PO} = F_V + 5.082138 \quad MHz$$

3 Calculate the standard (non-offset) pilot frequency (F_P) using the following formula.

$$F_P = F_{LCL} + 0.30944056 \quad MHz$$

Where: F_{LCL} = Lower channel limit frequency for the DTV channel.

4 Calculate the required pilot frequency offset (F_{OS}) using the following formula:

$$F_{OS} = F_{PO} - F_P$$

Where: F_P = The Standard (non-offset) DTV channel center frequency
F_{PO} = The pilot frequency with the required offset.

5 Enter the required offset frequency (F_{OS}) in the Main screen > Setup > Exciter Setup Freq. Offset field.

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Example:

A channel 38 DTV transmitter has a lower adjacent channel 37 NTSC transmitter within 88 km. Use the following procedure to determine its required offset pilot frequency.

1 The exact visual carrier frequency (F_V) is 609.25 MHz

2 The offset pilot frequency (F_{PO}) is:

$$F_{PO} = F_V + 5.082138 \text{ MHz}$$
$$= 609.25 + 5.082138 \text{ MHz}$$
$$= 614.332138 \text{MHz}$$

3 The standard (non-offset) pilot frequency (F_P) is:

$$F_P = F_{LCL} + 0.30944056 \text{ MHz}$$
$$= 614 + 0.30944056 \text{ MHz}$$
$$= 614.30944056 \text{MHz}$$

4 The pilot frequency offset (F_{OS}) is:

$$F_{OS} = F_{PO} - F_P$$
$$= 614332138 - 614309440.6 \text{ Hz}$$
$$= 22697.4 \text{ Hz}$$

6.1.1.2 Co-Channel DTV Transmitters

When Co-Channel DTV transmitters need to improve reception in a signal overlap area, interference rejection in receivers might be improved if one transmitter were offset in frequency by 1.5 times the DTV segment frequency (12.9353819 kHz), which equals 19.403 kHz. Both transmitters must be held to within +/- 10 Hz.

This offset, although specified by the ATSC A/64, has not currently been specifically authorized by the FCC. Since it offsets the DTV pilot more than 1 kHz, special FCC permission may be required before proceeding.

19403 Hz is the required offset frequency, so enter it in the Main screen > Setup > Exciter Setup Freq. Offset field.

6.1.1.2.1 Calculating New Pilot Frequency

The new pilot frequency will be needed. It can be calculated using the procedure below.

1 Calculate the standard (non-offset) pilot frequency (F_P) using the following formula.

$$F_P = F_{LCL} + 0.30944056 \text{ MHz}$$

Where: F_{LCL} = Lower channel limit frequency for the DTV channel.

2 Calculate the offset pilot frequency (F_{PO}) using the following formula.

$$F_{PO} = F_P + F_{OS}$$

Where: F_P = The Standard (non-offset) DTV channel center frequency
F_{PO} = The pilot frequency with the required offset
F_{OS} = The required pilot frequency offset.

Example:

WARNING: Disconnect primary power prior to servicing.

What is the new pilot frequency if the pilot is to be raised in frequency by 19.403 kHz.

1 The standard (non-offset) pilot frequency (F_P) is:

$$F_P = F_{LCL} + 0.30944056 \text{ MHz}$$
$$= 614 + 0.30944056 \text{ MHz}$$
$$= 614.30944056 \text{MHz}$$

2 Calculate the offset pilot frequency (F_{PO}) as follows:

$$F_{PO} = F_P + F_{OS}$$
$$= 614309440.6 + 19403 \text{ Hz}$$
$$= 614328843.6 \text{ Hz}$$

6.1.1.3 Co-Channel DTV and NTSC Transmitters

When there is signal overlap between an NTSC and a DTV transmitter on the same channel, any interference to the NTSC signal by the DTV signal would appear as noise, or snow, and would, in most cases, not be the major problem caused by signal overlap. The NTSC signal however, if strong enough, could disrupt DTV reception.

DTV receivers contain a switchable comb filter designed to reduce the strength of both NTSC carriers and the NTSC color subcarrier. To optimize the effect of the filter the DTV pilot frequency should be shifted to place the NTSC visual carrier near the null in the filter response.

This offset, although specified by the ATSC A/64, has not currently been specifically authorized by the FCC. The ATSC A/64 recommendation is to place the DTV pilot frequency 0.911944 MHz +/-1 Hz lower than the NTSC Visual Carrier frequency. Since the frequency tolerance of the offset is +/- 1 Hz, it is essential that both stations use precise frequency control.

This offset would place the DTV pilot well beyond the 1 kHz tolerance for the channel frequency. FCC approval may be needed in order to use this offset technique.

6.1.1.3.1 Possible NTSC Frequency Offsets

This is particularly important since the NTSC stations may have a +/-10 kHz offset to minimize NTSC to NTSC co-channel interference within their grade B signal overlap zones. To further minimize the overlap interference, the offset NTSC stations may have their visual carriers precisely controlled to a specific frequency, such as 10010 Hz or 10,489.51 Hz above or below the non-offset NTSC station.

6.1.1.3.2 Offset Calculation Procedure

1 Determine the exact visual carrier frequency (F_V) for the NTSC transmitter.

2 Calculate the offset pilot frequency (F_{PO}) using the following formula.

$$F_{PO} = F_V - 0.911944 \text{MHz}$$

3 Calculate the standard (non-offset) pilot frequency (F_P) using the following formula.

$$F_P = F_{LCL} + 0.30944056 \text{ MHz}$$

Where: F_{LCL} = Lower channel limit frequency for the DTV channel.

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4 Calculate the required pilot frequency offset (F_{OS}) using the following formula:

$$F_{OS} = F_{PO} - F_P$$

Where: F_P = The Standard (non-offset) DTV channel center frequency
F_{PO} = The pilot frequency with the required offset.

5 Enter the required offset frequency (FOS) in the Main screen > Setup > Exciter Setup Freq. Offset field.

Example:

A channel 38 DTV transmitter is experiencing interference from a co-channel NTSC transmitter. To determine its required pilot frequency offset (necessary to minimize the interference), the following procedure will be used.

1 The exact visual carrier frequency (F_V) for the NTSC is 615.25 MHz.

2 The offset pilot frequency (F_{PO}) is:

$$F_{PO} = F_V - 0.911944 = 615.25 - 0.911944 = 614.338056 \text{MHz}$$

3 The standard (non-offset) pilot frequency (F_P) is:

$$F_P = F_{LCL} + 0.30944056 \text{ MHz}$$
$$= 614 + 0.30944056 \text{ MHz}$$
$$= 614.30944056 \text{MHz}$$

4 The pilot frequency offset (F_{OS}) is:

$$F_{OS} = F_{PO} - F_P$$
$$= 614338056 - 614309440.6 \text{ Hz}$$
$$= 28615.4 \text{ Hz}$$

7 Parts List

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Table 7-1 EXCITER, APEX - 994 9912 001 (Modified)

Harris PN	Description	Qty UM	Reference Designators (G)
992 9995 035	*PWA, UHF EXTERNAL I/O	0.0 EA	ORDER QTY 1 FOR UHF OPERATION A7
992 9995 040	*PWA, VHF EXTERNAL I/O	0.0 EA	ORDER QTY 1 FOR VHF OPERATION A7
358 3579 000	SLIDES, DRAWER	1.0 PR	
398 0496 000	FUSE, SLOW CART 4A 250V	2.0 EA	
430 0288 000	BLOWER, 6-14VDC, 12V NOMINAL	1.0 EA	
448 1082 000	GASKET, EMI/RFI SHIELDING,	14.0 FT	#12.5' USED ON COVERS, 1.3' USED UNDER CENTER DIVIDER.
484 0446 000	FILTER, RFI POWER LINE ENTRY	1.0 EA	
484 0557 000	FILTER, LOWPASS, 750MHZ	1.0 EA	LPF001
556 0170 000	ATTEN, FIXED, 5DB 2W SMA	3.0 EA	# USED ON A5 DOWN CONVERTER. AT001 AT002 AT003
610 1253 000	MALE CONNECTOR, 4C,	1.0 EA	# USED WITH FAN CABLE
700 1422 019	LOAD, 50 OHM, 1/2W	1.0 EA	# USED ON 1 WATT AMP J3. A2J3
736 0356 000	POWER SUPPLY, 150W 4 OUTPUTS	1.0 EA	PS1
746 0257 000	LCD DISPLAY, 1/4 VGA COLOR	1.0 EA	
992 9995 002	*PWA, D/A CONVERTER	1.0 EA	A12
992 9995 004	*PWA, FRONT PANEL	1.0 EA	A10
992 9995 006	PWA, DOWN CONVERTER	1.0 EA	A5
992 9995 008	*PWA, CONTROLLER	1.0 EA	A8
992 9995 011	*PWA, A/D CONVERTER	1.0 EA	A11
992 9995 013	*PWA, ADAPTIVE PRECORRECTOR	1.0 EA	A9
992 9995 015	PWA, UDC INTERFACE	1.0 EA	A6
901 0121 061	PWA, PLL	1.0 EA	A4
992 9995 022	*PWA, MODULATOR	1.0 EA	A13
992 9995 024	PWA, OUTPUT AMPLIFIER	1.0 EA	A2
992 9995 028	*PWA, SMPTE-310M INTERFACE	1.0 EA	A14
992 9995 030	PWA, UPCONVERTER	1.0 EA	A3
992 9995 033	PWA, UHF BAND PASS FILTER	1.0 EA	

WARNING: Disconnect primary power prior to servicing.

2604sapa.fm

Appendix A Exciter GUI Screen Captures

This is the screen capture procedure, using Tera Term Pro, for the APEX FLO exciter.

1 Connect a male-female DB-9 straight-through cable from Com 1 on your computer to the RS232 connector on the front or rear panel of the APEX FLO exciter.

2 Open Tera Term Pro on the computer.

3 Select “Setup > Serial port”.

- A Set the serial port parameters to match the exciter RS232 parameters for the exciter port which is connected to the computer. This information can be found at Setup > Serial I/O > Serial Setup 1/3 RS-232 screen on the exciter GUI screen. The protocol must be VT100.
- B Hit OK to accept the setup.

4 Press Enter twice in rapid succession to access the exciter. If connection is successful, a screen similar to that shown in Figure A-1 should appear.

- A The screen capture function is on page 1 of 7 when viewed on the computer. If any other page or a blank screen appears, the screen capture function will not operate. Use the left or right arrow key to change to the correct page.

5 On the exciter GUI, select the screen to be captured.

6 On the Tera Term program, enter d, but **do not hit** any other key as prompted. The location and file name for the screen capture must be entered first, continue with step 7.

7 On the Tera Term program, select File > Log.

- A Select the directory for the screen capture file.
- B Enter the file name.bmp for the screen to be captured.
- C In the Options sub window, select Binary and do not select Append.
- D Press Open.

8 Hit any key and the screen download will proceed. A scrolling of information, similar to that of Figure A-2, will occur while the download in progress.

9 When the download is complete (the scrolling stops) the log file must be closed.

- A Select the Tera Term Log tab at the bottom of the computer screen, a window similar to that shown in Figure A-3 will appear.
- B The Bytes Transferred entry should indicate 77878 bytes. Any other size represents an error and the screen download has failed.
  1. If smaller, most likely there was an error in the data transfer. The screen shot will probably be legible but will have a “smear” or tear in the bitmap.
  2. If larger, an error probably occurred in downloading and setting up the log file. Set up the log file AFTER pressing “D” for screen capture, while the window says “press any key to start screen capture”.
  3. If the number is 77879 instead of 77878, echo is enabled in the terminal program and it caught the key stroke at the beginning of the screen dump. In the Setup > Terminal window, make sure the local echo box is not checked.
- C Press the close soft key to close the log file.

10 If you want to capture another screen after closing the log file, select “Control” and then “Reset terminal”. Press “Enter” twice and return to step 5 to capture another screen.

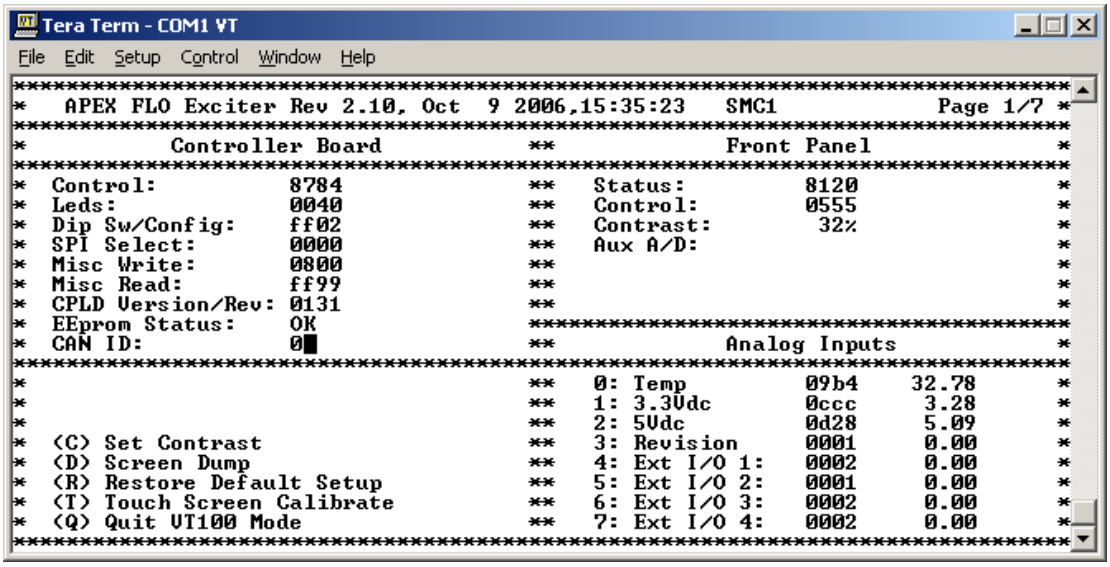

Figure A-1 Tera Term Pro Screen When Connected to Exciter

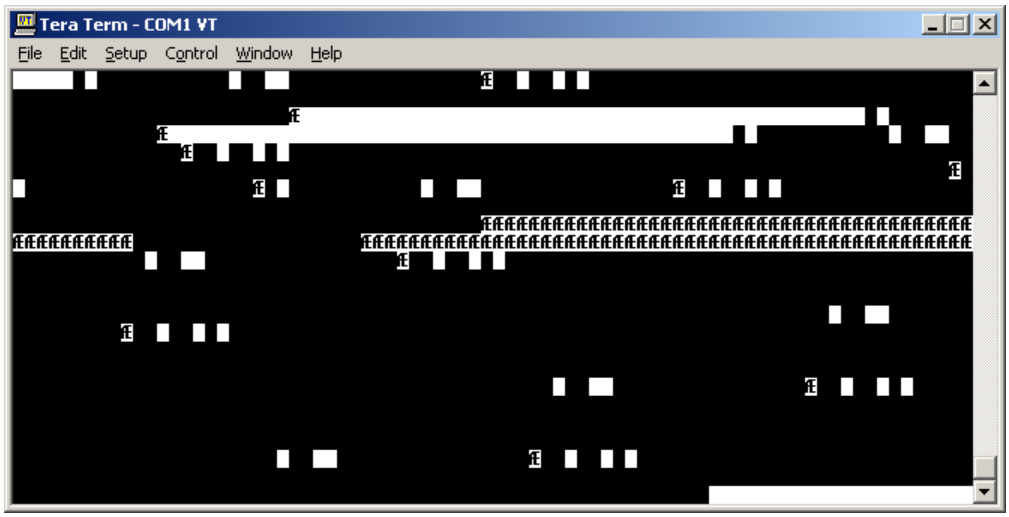

Figure A-2 Stop Action Capture of Screen Down Load Scroll.

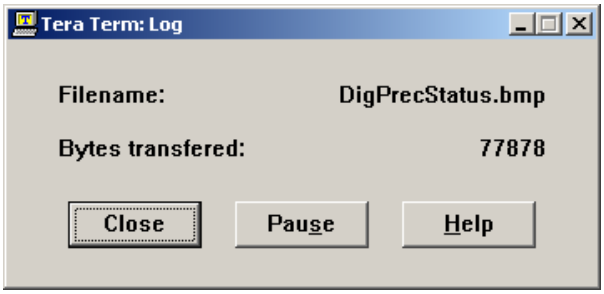

Figure A-3 Tera Term Log Window Selected When Download Has Completed